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A G-Band Frequency Doubler Using a Commercial 150 nm GaAs pHEMT Technology

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Abstract

This paper presents a frequency doubler operating at G-band that exceeds the maximum oscillation frequency (f_{max}) of the given transistor technology. A common-source transistor is biased on class-B to obtain sufficient output power at the second harmonic frequency. The input and output impedances are matched to achieve high output power and high return loss. The frequency doubler is fabricated in a commercial 150-nm GaAs pHEMT process and obtains a measured conversion gain of −5.5 dB and a saturated output power of −7.5 dBm at 184 GHz.

Key Words: Frequency Doubler, G-Band, GaAs pHEMT, Harmonic Matching.

I. INTRODUCTION

A signal source is one of the essential circuit blocks used for high-resolution imaging or high-speed wireless communication at mm-wave and terahertz bands. However, designing a fundamental oscillator at such a high frequency remains challenging because of the limitation of transistor speed, which is usually quantified by a maximum oscillation frequency (f_{max}).

Instead of a fundamental oscillator, harmonic oscillators and frequency multipliers [1–4] have been widely used for signal generation at a high frequency that is close to f_{max}. With the advancements in transistor technology, several frequency doublers operating at hundreds of GHz have been reported recently [5–9]. However, they mostly utilize advanced semiconductor processes, which may suffer from high cost and limited accessibility.

In this paper, we implement a G-band frequency doubler using a relatively low-cost commercial 150-nm GaAs pHEMT technology. This technology is not optimum for the doubler design because the transistor f_{max} is only 160 GHz, which is lower than the doubler operation frequency. However, the transistor topology, bias condition, and impedance matching are optimized to obtain sufficient output power at G-band. The proposed frequency doubler demonstrates the feasibility of implementing a low-cost terahertz source based on a less-advanced transistor technology.

II. G-BAND FREQUENCY DOUBLER DESIGN

To determine the optimum structure for the frequency doubler, the second-harmonic output power of three different transistor topologies, namely, common-gate (CG), common-source (CS), and cascode, are compared, as shown in Fig. 1. The input power is fixed to 0 dBm, and no impedance matching is considered in each topology. As frequency increases, the output power of cascode and CS gradually reduces. Specifically, the decrease

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in cascode power is more pronounced because the cascode transistor presents loss rather than gain beyond f_{max} of the transistor. Therefore, the cascode topology is excluded in this G-band frequency doubler.

On the other hand, the output power of CG increases with frequency. At the target frequency of 220 GHz, CG generates a 2.5-dB higher output power than CS. However, it should be noted that no impedance matching is considered in the simulation of Fig. 1. Therefore, determining the optimum topology between CS and CG is not yet straightforward.

For a more practical comparison, the second-harmonic power is re-simulated while the input and output impedances are matched to 50 Ω at 110 and 220 GHz, respectively. As expected, cascode exhibits the lowest output power in Fig. 2. CS and CG generate comparable output power at a low input level. However, the saturated power of CS is considerably higher than that of CG. Although CG can benefit from a better bandwidth than CS because of wider input matching, we still choose the CS topology to obtain higher output power.

A schematic of the G-band frequency doubler is illustrated in Fig. 3. A single-stage CS structure with simple stub matching is employed to minimize the effect of device model inaccuracy at high frequency. The gate width of the transistor is determined as 2 × 25 μm, which yields the highest second-harmonic power at 220 GHz.

The gate bias voltage (V_{gs}) is also selected to maximize the second-harmonic power. Fig. 4 shows the simulated drain current at the fundamental and second-harmonic frequencies versus V_{gs}. The drain bias voltage (V_{ds}) is fixed to 1 V. The second-harmonic current has two peaks at V_{gs} = –1.1 V and –0.2 V. Although showing a higher current at 220 GHz, the peak at V_{gs} = –0.2 V is avoided because of its large DC power consumption and high harmonic generation. Therefore, the other peak at V_{gs} = –1.1 V is chosen. Furthermore, this class-B bias condition brings the advantage of zero DC power consumption when no RF input is applied.

Through a harmonic load-pull simulation, the optimum output impedance yielding the maximum second-harmonic power is obtained. The impedance turns out to be close to the conjugate matching impedance. Therefore, the output is conjugately matched at 220 GHz to achieve high output power and high return loss. The input is also conjugately matched at 110 GHz.

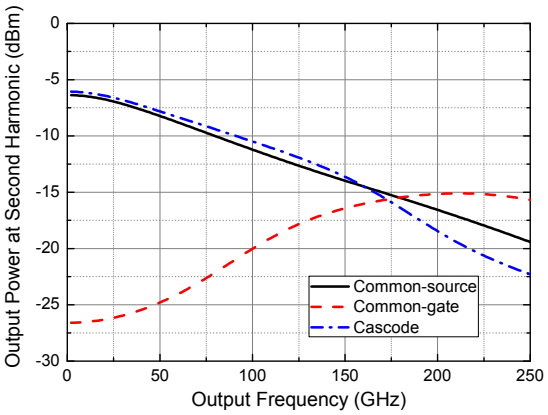

Fig. 1. Comparison of second-harmonic output power among three different transistor topologies at P_{in} = 0 dBm.

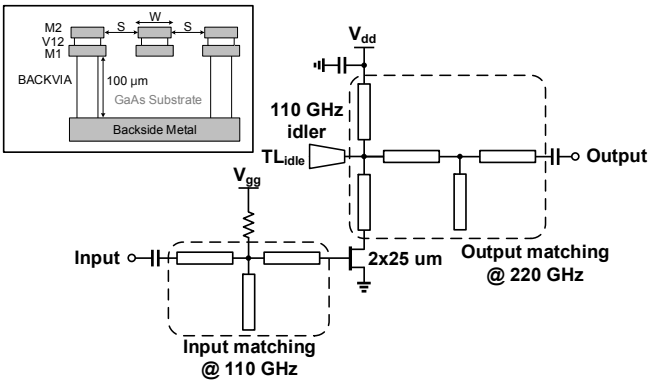

Fig. 3. Schematic of the G-band frequency doubler.

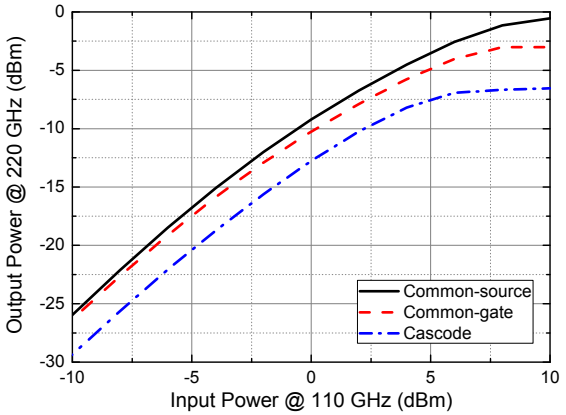

Fig. 2. Comparison of output power at 220 GHz versus input power at 110 GHz among three different transistor topologies.

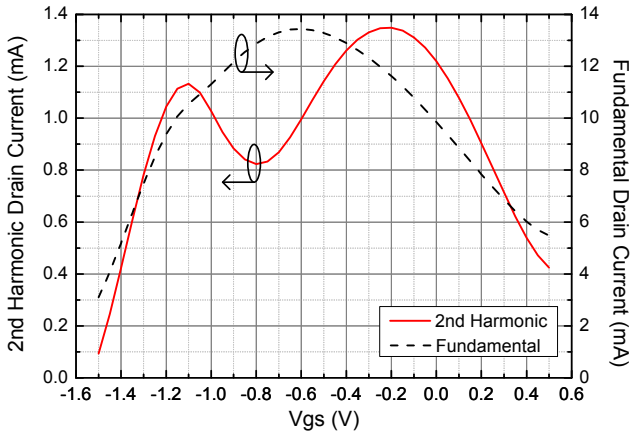

Fig. 4. Simulated drain currents at the fundamental and second-harmonic frequencies versus V_{gs} (V_{ds} = 1 V).

A radial stub is inserted into the output to suppress the fundamental component. The input and output matching network is implemented using a CPW structure, as shown in the inset of Fig. 3. Compared with a microstrip line, CPW benefits from a relatively low radiation loss and a narrow line width. The width (W) and spacing (S) for a 50-Ω characteristic impedance are 15 μm and 10.5 μm, respectively. All CPW lines are simulated using a commercial electromagnetic (EM) simulator (Agilent Momentum).

Fig. 5 shows the simulated port matching performance. The return loss at the input and output is higher than 10 dB at 110 GHz and 220 GHz, respectively. Fig. 6 shows the simulated conversion gain and fundamental suppression versus output frequency when the input power is 2 dBm. The conversion gain is −14.5 dB at 220 GHz, and the fundamental component is suppressed by more than 20 dB at the output.

III. Measurements

The G-band frequency doubler was fabricated in a commercial 150-nm GaAs pHEMT process. The transistor f_{max} is 160

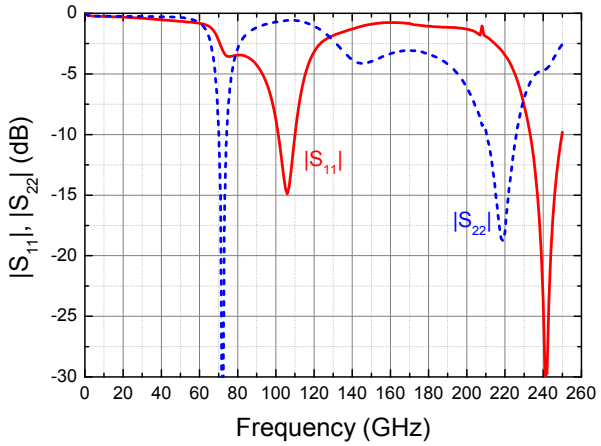

Fig. 5. Simulated input and output matching performance.

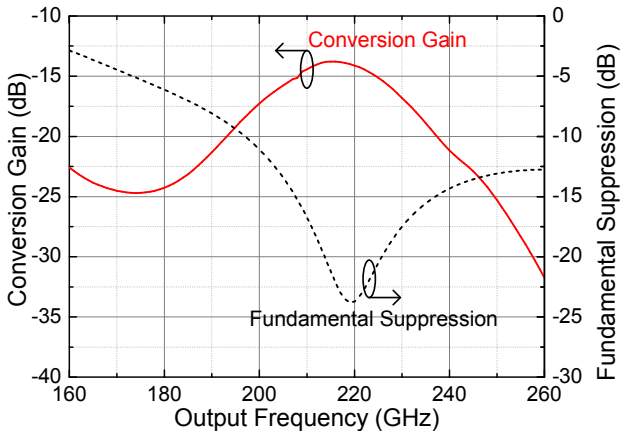

Fig. 6. Simulated conversion gain and fundamental suppression versus output frequency at P_{in} = 2 dBm.

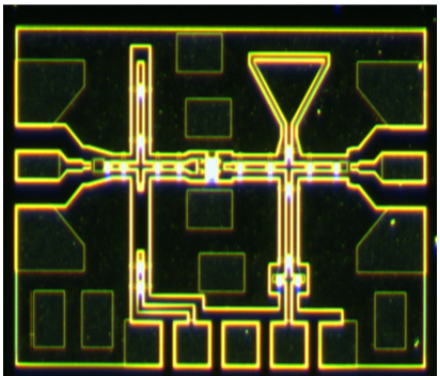

Fig. 7. Chip micrograph of the G-band frequency doubler (1.0 mm × 0.63 mm).

GHz, which is considerably below the operating frequency of the frequency doubler. Fig. 7 shows a chip micrograph, which occupies an area of 1.0 mm × 0.63 mm.

The chip is measured with a waveguide-based on-chip probing setup, as shown in Fig. 8. The input signal is generated by a W-band source module with a built-in variable attenuator. The chip is probed by waveguide probes and sections. The output power is measured with a calorimeter-based power meter. The loss of waveguide probes and sections, as indicated in Fig. 8, are de-embedded in the measurement.

Fig. 9 shows the measured conversion gain versus the output frequency when the input power is −16 dBm. A peak conversion gain of −5.5 dB is measured at 184 GHz. The conversion gain is higher than −7.6 dB from 180 GHz to 196 GHz. Compared to simulation (long-dashed line), the operating frequency is shifted down and the gain increases. This is presumably due to the underestimation of the electrical length of CPW lines. Therefore, we perform additional simulation with extra length considered. The post-simulation result (short-dashed line) becomes closer to the measurement. A residual discrepancy is due to the inaccuracy of the transistor model at the frequency above transistor f_{max}.

Fig. 10 shows the measured output power and conversion

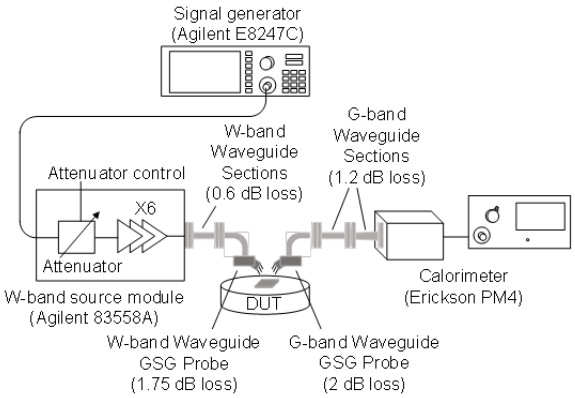

Fig. 8. On-chip power measurement setup for the G-band frequency doubler.

Table 1. Comparison of this work with other millimeter wave frequency multipliers

	This work	[2]	[4]	[5]	[6]	[7]	[8]	[9]
Frequency f_{out} (GHz)	180–196	92.5–96.5	DC–100	150–220	200–235	250–310	138–170	170–190
Conversion gain (dB)	−5.5	-	−3	3	−7	-	4.9	−6.4
Saturated output power (dBm)	−7.5	3	−8	−6	−4	−6.4	5.6	0
Technology	150-nm GaAs pHEMT	100-nm GaAs HEMT	InP DHBT	50-nm GaAs mHEMT	50-nm mHEMT	50-nm mHEMT	130-nm SiGe HBT	45-nm SOI CMOS
f_T, f_{max} (GHz)	85, 160	>100, -	180, 220	-, 380	380, 380	400, 420	300, 500	200, -
f_{out} / f_{max} ratio	1.15	-	0.45	0.47	0.57	0.67	0.31	-

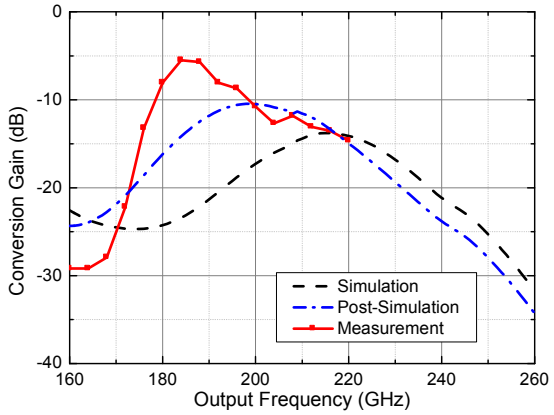

Fig. 9. Measured conversion gain at P_{in} = −16 dBm.

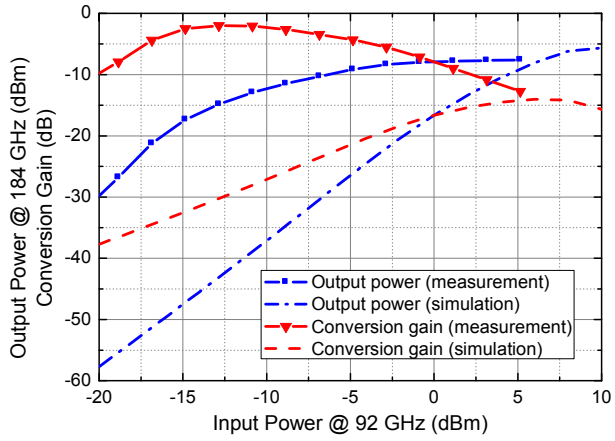

Fig. 10. Measured output power and conversion gain at 184 GHz versus input power.

gain at 184 GHz as the input power increases from −20 dBm to 5 dBm. The maximum output power is −7.5 dBm. The discrepancy between the simulation and measurement is also due to the inaccuracy of the transistor model and EM simulation. The DC drain current flows 2.6 mA at V_{ds} = 1 V when an RF input power of 5 dBm is applied.

The frequency doubler is compared with other reported mm-wave frequency multipliers operating at similar frequencies in Table 1. The saturated output power and conversion gain are comparable with those of other works. However, it should be noted that all other multipliers were fabricated in advanced and (or) research-oriented processes that offer excellent transistor f_{max} above 220 GHz. Conversely, the frequency doubler in this work utilizes a low-cost commercial process offering low transistor f_{max}, even lower than the operating frequency. The ratio of output frequency to transistor f_{max} exceeds unity only in this frequency doubler.

IV. Conclusion

In this paper, a G-band frequency doubler is demonstrated using a commercial 150-nm GaAs pHEMT process offering transistor f_{max} lower than the operating frequency. The measurements show that the conversion gain is −5.5 dB and the saturated output power is −7.5 dBm at 184 GHz. The conversion gain is no lower than −7.6 dB over the frequency from 180 GHz to 196 GHz. The frequency doubler can be used as a low-cost terahertz source for imaging and wireless communication.

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