SAR ADC for a Multimode Radar Transceiver with Offset Calibration
Jin-Seop Lee · Hyun-Yeop Lee · Choon-Sik Cho* · Young-Jin Kim

Abstract

In this paper, we design a successive approximation register (SAR) analog-to-digital converter (ADC) suitable for multimode radar transceivers. For multimode radars, the sampling rate required by ADC varies according to the continuous wave (CW) or frequency modulated continuous wave (FMCW) used for operation. Therefore, depending on which waveform is used, the input is designed to enter two paths. For path 1, we obtained 9.23 bits of effective number of bits (ENOB), 57.35 dB of signal-to-noise distortion ratio (SNDR), and 64.62 dB of spurious free dynamic range (SFDR), and the power consumption was 0.3481 mW, resulting in a figure of merit (FOM) of 28.9 fJ/Conv-Step. On path 2, we obtained an 8.97 bit of ENOB, 55.76 dB of SNDR, and 60.53 dB of SFDR, and the power consumption was 1.72 μW, resulting in a FOM of 34.2 fJ/Conv-Step. Further, a circuit was constructed to reduce the offset of the comparator. As a result of 100 Monte Carlo simulations, the offset was reduced from -46 mV/+50 mV to -4 mV/+4 mV when the worst case was considered.

Key Words: FMCW, CW, multimode radar, SAR ADC, offset calibration.
is designed as NMOS, as shown in Fig. 1, and Eq. (2) shows the error in the output of the sample-and-hold considering the charge injection.

\[
R_{ON} = \frac{1}{(\mu C_{on} W / L)(V_{GS} - V_{TH})} 
\]

\[
\Delta V = \frac{WLC_{ox}(V_{DD} - V_{in} - V_{TH})}{2C_H} 
\]

Eq. (1) and Eq. (2) show that there is a trade-off relationship between Ron and charge injection, depending on the size of the switch [4]. Fig. 2 shows the spurious free dynamic range (SFDR) according to the input frequency and size of the CMOS switch. The sampling rate is based on Nyquist sampling. If the sampling rate is high, the larger switch provides a higher signal-to-noise distortion ratio (SNDR), and if the sampling rate is low, the smaller switch provides a higher SNDR.

Therefore, in this work, when using FMCW, the switch's clock was bootstrapped, and the sampling capacitor was used separately. When using CW, a small switch was used, and CDAC was designed to act as a capacitor for the sample-and-hold circuits.

Further, the DC offset of ADC, which causes errors in distance or speed, is eliminated primarily by signal processing in DSPs; however, in this work, we designed circuits that calibrate offset in analog-integrated circuits. In general, offset calibration in the comparator includes auto-zeroing [5], which is a method of sampling offset charge, or a method of compensating Vth mismatch by changing the body voltage on both sides of the input MOSFET through a charge pump and phase detector [6].

However, in the case of auto-zeroing, the SAR ADC requires a preamp with a high gain, which slows the ADC’s operating speed. The disadvantage of changing body voltage is that if the offset is too large, too much change in body voltage can lead to leakage from the body to the source or body to drain, and the addition of a switch used in offset calibration mode slows the capacitor down. To overcome these shortcomings, this paper calibrates offset using a method of changing V_{ref}.

The remainder of this paper is organized as follows: Section II describes the structure of the proposed ADC and the description of each block, Section III describes the simulation results, and Section IV concludes this paper.

II. ARCHITECTURE AND CIRCUIT DESCRIPTION

Fig. 3 shows the block diagram of the SAR ADC. First, in the offset calibration phase, the SAR control logic does not work, and the offset of the comparator is calibrated. As shown in Eq. (3), the offset can be reduced if the input MOSFET is large [7].

\[
v_{\text{offset}} = \left(\frac{W}{L} \cdot \frac{\Delta V_{T,H}}{2} \right) + \left(\frac{W}{L} \cdot \frac{\Delta V_{T,L}}{2} \right) + \left(\frac{W}{L} \cdot \frac{\Delta V_{T,P}}{2} \right) \right)^2
\]

However, there are two disadvantages to designing an input MOSFET large. First, the kickback noise caused by the clock of the comparator increases. Second, the CDAC produces a gain error equal to \(C_3/(C_3 + C_P)\). In particular, the size of the sampling capacitor used in the FMCW mode was smaller in this work, which is more fatal. Therefore, the size of the input MOSFET is designed to be calibrated instead of the small size of the input MOSFET designed to be calibrated.
In the A/D conversion phase, the offset calibration logic does not work, and the differential input signal enters two paths, and the magnitude of the output voltage at paths 1 and 2 determines the output of the comparator. In the FMCW mode, the input enters path 1, and the input switch in path 2 is designed to always be open. At this point, the sampled input in path 1 is output, and at path 2, the voltage that is feedback through the comparator, control logic, and CDAC is output. Conversely, in the CW mode, the input enters path 2, the input switch in path 1 is always open, and the output of path 1 is always designed to be common-mode voltage (VCM). In path 2, the sampled input and the voltage from the CDAC are added to the output. In both paths 1 and 2, input is sampled using the bottom plate sampling technique, in CDAC in path 2, VCM based switching is used to reduce area and energy consumption, and a bridge capacitor is used. Further, in path 1, the switch uses a bootstrap circuit to sample fast inputs, and in path 2, a transmission gate switch with a simpler structure and less power consumption than the bootstrap circuit is used because it does not sample fast inputs.

Fig. 4 shows a schematic of the bootstrap circuit. In the track-and-hold circuit, the sampling speed is determined by the value of the \( R_{\text{on}} \) of the MOSFET and the value of the sampling capacitor. If only a simple NMOS is used as a switch, it causes nonlinearity that changes \( V_{\text{th}} \) according to \( V_{\text{in}} \). However, the use of bootstraps can prevent \( R_{\text{on}} \)'s value from changing as \( V_{\text{in}} \) changes by fixing the value of \( V_{\text{gs}} \) [8]. However, as shown in Eq. (4), the change in \( V_{\text{th}} \) caused by the body effect follows the change in \( V_{\text{in}} \).

\[
V_{\text{th}} = V_{\text{th0}} + \gamma (\sqrt{2F} + V_{\text{sh}} - \sqrt{2F})
\]

(4)

The change in \( V_{\text{th}} \) causes a change in \( R_{\text{on}} \) and a change in charge injection [9]. To prevent the \( V_{\text{th}} \) from changing due to the body effect, the body is connected to the \( V_{\text{in}} \) during the sampling phase. In the hold phase, the body is connected to the ground to prevent leakage from the body to the output.

Fig. 4. Schematic of the bootstrap circuit.

Fig. 5 is a schematic of the comparator designed with 4 inputs based on a double tail current comparator [10]. The double-tail current comparator is more advantageous than the commonly used strong-arm latch in terms of current consumption, delay, and offset compared to the commonly used strong-arm latch.

Fig. 5. Schematic of the comparator.

Fig. 6 shows a circuit diagram of the CDAC. VCM-based switching technique is used to reduce the area and switch energy consumption, and the total area is greatly reduced using bridge capacitors [11]. The size of the bridge capacitor is equal to that of the unit capacitor.

Fig. 6. CDAC with a split capacitor.

Fig. 7 shows a block diagram of the offset calibration. We propose a method for offset calibration by controlling the reference voltage according to the output result of the comparator in the offset calibration phase. If offset is present, the action is to bring the values of \( V_{\text{refp}} \) close to \( V_{\text{refp}} + V_{\text{offset}} \), as shown in Fig. 8.

Fig. 7. Block diagram of the offset calibration.

Fig. 9(a) shows a circuit diagram of the offset control logic, and Fig. 9(b) shows a circuit diagram of the reference voltage...
with the switch. If offset is present, the offset is compensated by increasing $V_{ref,n}$ or $V_{ref,p}$ according to the output of the comparator. Fig. 10 shows $V_{ref,n}$ following $V_{ref,p}$ when the offset is modeled at 10 mV using an ideal source of voltage without a mismatch.

Before and after calibration, a Monte–Carlo simulation was carried out to check the offset of the capacitor. As shown in Fig. 11, the offset of the comparator before calibration was $-46$ mV and $50$ mV in the worst case. By contrast, after calibration, the offset was $-4$ mV and $4$ mV in the worst case. Table 1 compares offsets before and after calibration.

<table>
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<tr>
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<th>Before calibration</th>
<th>After calibration</th>
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<tbody>
<tr>
<td>Mean of Absolute offset [mV]</td>
<td>14.78</td>
<td>1.54</td>
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<tr>
<td>Min offset [mV]</td>
<td>$-46$</td>
<td>$-4$</td>
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<tr>
<td>Max offset [mV]</td>
<td>50</td>
<td>4</td>
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### III. SIMULATION RESULT

Fig. 12 shows the results of the fast Fourier transform (FFT) simulation of the designed ADC. This result is a pre-simulation result, but a capacitance of 5 fF was applied to the intermediate node of each block in consideration of the value of parasitic capacitance that may occur during the layout. Fig. 12(a) is
obtained when the input enters path 1, and the input frequency is determined to be close to 10 MHz, considering coherent sampling. Fig. 12(b) shows that the input enters path 2, and the input frequency is similarly determined to be around 50 kHz, considering coherent sampling. Simulation results show that if the input enters path 1, it obtains an SFDR of 64.62 dB, an SNDR of 57.35 dB, and an effective number of bits (ENOB) of 9.23 bits. Power consumption is 0.3481 mW, and FOM is 28.9 fJ/Conv-Step. If the input enters path 2, it obtains an SFDR of 60.53 dB, an SNDR of 55.76 dB, and an ENOB of 8.97 bits. Power consumption is 1.72 μW and FOM is 34.2 fJ/Conv-Step.

Table 2. Comparison of SAR ADC with a comparable sampling rate when using path 1

<table>
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<td>Technology [nm]</td>
<td>65</td>
<td>65</td>
<td>130</td>
<td>130</td>
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<tr>
<td>Supply Voltage [V]</td>
<td>1.2</td>
<td>0.6</td>
<td>1.2</td>
<td>1.2</td>
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<td>Resolution [bit]</td>
<td>10</td>
<td>12</td>
<td>10</td>
<td>12</td>
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<tr>
<td>Sampling rate [S/s]</td>
<td>20M</td>
<td>10M</td>
<td>50M</td>
<td>40M</td>
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<tr>
<td>SNDR [dB]</td>
<td>57.35</td>
<td>64.3</td>
<td>52.8</td>
<td>62.5</td>
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<tr>
<td>SFDR [dB]</td>
<td>64.62</td>
<td>83.8</td>
<td>-</td>
<td>73</td>
</tr>
<tr>
<td>ENOB [dB]</td>
<td>9.23</td>
<td>10.4</td>
<td>8.48</td>
<td>10.08</td>
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<tr>
<td>Power [mW]</td>
<td>0.3481</td>
<td>0.083</td>
<td>0.92</td>
<td>1.32</td>
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<tr>
<td>FOM [fJ/Conv-Step]</td>
<td>28.9</td>
<td>6.2</td>
<td>52</td>
<td>30.4</td>
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</table>

(* pre-simulation result)

Table 3. Comparison of SAR ADC with comparable sampling rates when using path 2

<table>
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<td>10</td>
<td>10</td>
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<tr>
<td>Sampling rate [S/s]</td>
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<td>10K</td>
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<td>1K</td>
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<tr>
<td>SNDR [dB]</td>
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<td>60.5</td>
<td>60.4</td>
<td>56.5</td>
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<tr>
<td>SFDR [dB]</td>
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<td>72</td>
<td>69.2</td>
<td>75.3</td>
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<tr>
<td>ENOB [dB]</td>
<td>8.97</td>
<td>9.76</td>
<td>9.75</td>
<td>9.1</td>
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<tr>
<td>Power [μW]</td>
<td>1.72</td>
<td>0.25</td>
<td>8.25</td>
<td>0.0058</td>
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<tr>
<td>FOM [fJ/Conv-Step]</td>
<td>34.2</td>
<td>28.8</td>
<td>95.8</td>
<td>10.94</td>
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</table>

(* pre-simulation result)

IV. CONCLUSION

This paper shows the design results in the TSMC 65nm process and uses a supply voltage of 1.2 V. We designed a suitable SAR ADC for multimode radar transceivers. In both modes, inputs are designed to fit in different paths, both with a resolution of 10 bits. The ADC was designed to operate at sampling rates of 20MS/s and 100KS/s, respectively, and when Nyquist sampling was performed, path 1 obtained an SFDR of 64.62 dB, an SNDR of 57.35 dB, and an ENOB of 9.23 bits. Power consumption was 0.3481 mW, and FOM was 28.9 fJ/Conv-Step. In the case of path 2, SFDR was 60.53 dB, SNDR was 55.76 dB, ENOB was 8.97 bits, power consumption was 1.72 μW and FOM was 34.2 fJ/Conv-Step. The design also configured a
circuit for offset calibration of the comparator to reduce the offset from -46 mV/+50 mV to -4/+4 mV in the worst case.

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REFERENCE


Jin-Seop Lee received his B.S. and M.S. degrees from the Department of Electrical Engineering, Korea-Aerospace University, Go-yang, Korea, in 2020 and 2022, respectively. His research interests include the design of RFIC, data converters, and radar systems.

Choon-Sik Cho received his B.S. in Control and Instrumentation Engineering from Seoul National University in 1987, his M.S. in Electrical and Computer Engineering from the University of South Carolina in 1995, and his Ph.D. in Electrical and Computer Engineering from the University of Colorado in 1998. From 1987 to 1993, he worked at LG Electronics with a focus on communication systems. From 1999 to 2003, he worked for Curitel, where he was principally involved in the development of mobile phones. He joined the School of Electronics and Information Engineering at Korea Aerospace University in 2004. His research interests include the design of RFIC/MMIC, millimeter-wave ICs, analog circuits, and radar systems.

Hyun-Yeop Lee received his B.S. degrees from the Department of Electrical Engineering, Korea Aerospace University, Go-yang, Korea in 2021. His research interests include the design of RFIC, data converters, and radar systems.

Young-Jin Kim received his B.S. degree in electrical engineering from Kyung-pook National University in 1995. He received M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST) in 1997 and 2002, respectively. His Ph.D. dissertation focused on the transceiver architecture of image rejection and spurious rejection. In 2002, he joined Samsung Electronics, Co., Ltd., Korea, as a senior engineer. Since then, he has participated in the design of CDMA and GSM/GPRS wireless mobile applications. Furthermore, he designed an LNA and down-conversion mixer for multimode CDMA and GSM/GPRS. In 2006, he joined the School of Electronics and Information Engineering, Korea Aerospace University, Go-yang, Korea.