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Design of a 0.5–18 GHz Wideband Frequency Down-Converter Module with a Local Circuit for an Electronic Support Measurement System

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Abstract

In this paper, we describe the design and fabrication of a wideband frequency down converter module that has a local circuit with high gain, low spurious, high IP3 (3rd intercept point) characteristics, and reliability; this is accomplished by applying a chip-and-wire process using a bare type monolithic microwave integrated circuit (MMIC) device. To compensate for the mismatch among many sub-modules, an input module, filter bank module, output module, and local oscillator (LO) module suitable for sub-band frequency characteristics were designed and applied to the down converter. The frequency down converter module had three paths: 0.5–2 GHz (direct), 2–6 GHz (direct), and 6–18 GHz (converter). Amplitude-matched radio frequency (RF) semi-rigid cables of different lengths were used to connect to the internal sub-modules of the frequency down converter. The main RF line was a dielectric substrate, RT/duroid 5880, with a relative dielectric constant of 2.2 and a dielectric thickness of 0.127 mm. In the wideband frequency down converter module, the gain was 22.7 dB at low band (input frequency, 0.5–2 GHz) with a flatness of about 3.4 dB. The gain was 22.6 dB at mid band (input frequency, 2–6 GHz) having flatness about 2.0 dB. The gain was from 30 dB at edge frequency of high band (input frequency, 14–18 GHz) with a flatness of about 4.2 dB. The measured value of IP3 at LB was +23.52 dBm, +25.66 dBm and +23.44 dBm as the maximum value. The measured value of spurious (LO-2IF) at the converter path was 34.97 dBc as the maximum value.

Key Words: Chip-and-Wire, ESM System, Frequency Down Converter, Front-End, Local Circuit, Low Spurious, Wideband.

I. Introduction

The modern electronic warfare (EW) environment is characterized by emitter systems, which are increasing in number and sophistication. To protect humans and equipment and communicate effectively in an electro-magnetically threatening signal environment, acquisition receivers capable of analyzing several simultaneous threat signals that may be distributed over a wide band of frequencies are essential [1].

An electronic support measurement (ESM) module is described that meets these requirements and provides a dual channel architecture with close amplitude and phase matching is described in this paper. The module may be used not only as a generic front-end for conventional ESM applications but also for mono-pulse or interferometry techniques. The amplitude and phase match that can be achieved be-tween the channels are the fundamental limitations to the accuracy of bearing assessment for direction-finding (DF) techniques [2].

Although numerous studies have been conducted to design millimeter-wave ultra-wideband receivers suitable for electronic

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support systems, there are many constraints on the design and manufacturing of such broadband down converters such as wire bonding accuracy, printed circuit board (PCB) attachment tolerance. To produce receivers with low noise figures, smooth gain characteristics in the band, wide dynamic ranges, and band-specific frequencies with low-loss transmission lines. A local oscillator circuit necessary for frequency conversion should be incorporated into the module, and a closed structure is required to avoid signal interference from other devices—identification, friend or foe (IFF) transponder, Doppler radar, communication system, etc.—in the system environment in which the receivers are installed [3, 4].

The direction of arrival (DOA) of an RF signal can be determined from amplitude measurements taken when scanning a high-gain parabolic dish antenna with low side lobes across the direction of the emitter. The most common approach to amplitude comparison DF is to use four low-gain steady antennas displaced 90° from each other to provide four angular quadrants of azimuth coverage. The arrangement of the four antennas is shown in Fig. 1 [5].

The concept for considering the operation scenario within the electronic support system was constructed so that the front-end modules were installed in the east, west, south, and north to allocate 90° to each, enabling signals to be received across 360° as shown in Fig. 2. When a signal received in a specific direction is detected, only signals received from corresponding path are precisely analyzed.

The module gain was required at the system level (from the front-end to signal processing) in advance and was predicted to allocate an appropriate gain for each device. The insertion loss of a 15-m cable in the middle of the device was included among

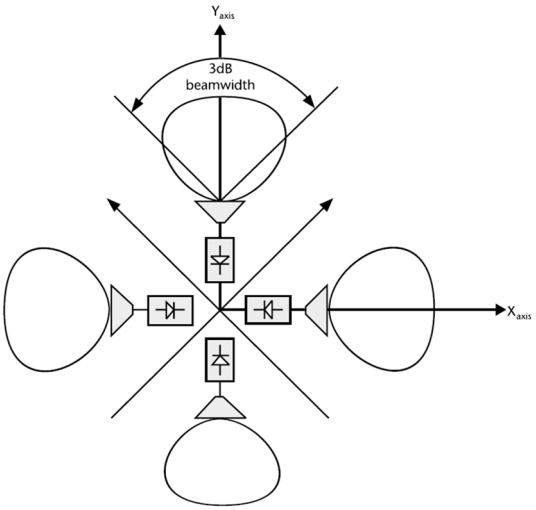


Fig. 1. Arrangement of the four antennas for direction-finding amplitude.

the analysis items in the consideration of the structure to be mounted. To compensate for increased loss value as the frequency of the RF cable increases, a linear equalizer is applied so that the gain is relatively low at a low frequency.

The device to be developed in this paper is an FE module mounted at the rear of the antenna, the frequency plan of which shown in Table 1. This is required to distinguish between direct paths or converting paths to prevent mutual influence between the frequencies introduced in each path. To efficiently down-convert 0.5–18 GHz received over a wideband, 0.5–2 GHz is output without conversion, and 2–18 GHz is mixed with a local oscillation (LO) frequency to be converted into a 2–6 GHz intermediate frequency (IF) signal as shown in Table 1.

In addition, because strict out-of-band suppression character-

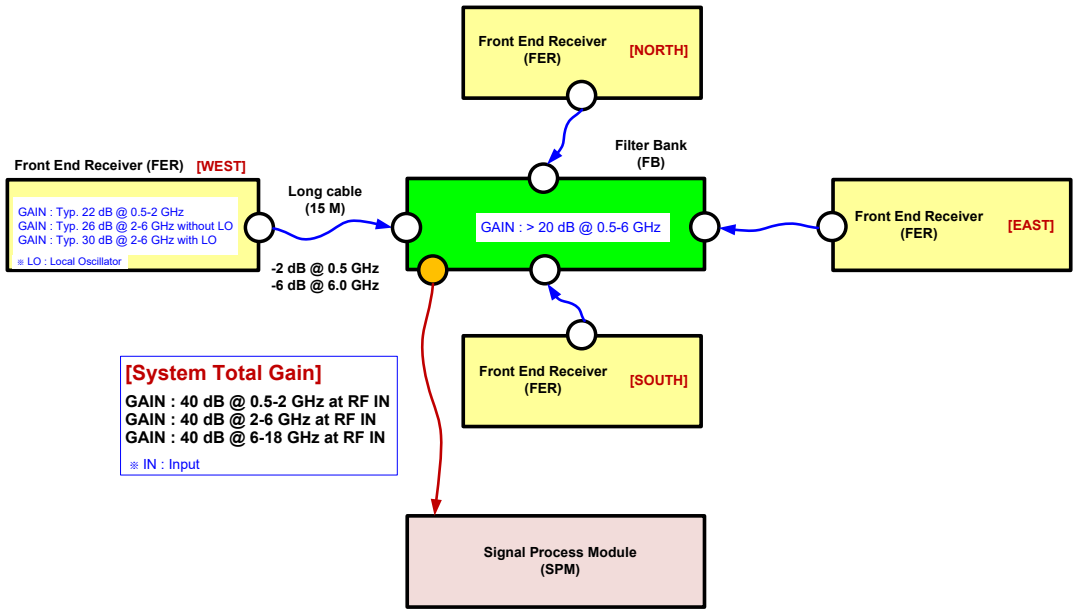


Fig. 2. Block diagram of system total gain for front end receiver (4 units) and filter bank (1 unit) from operation scenario point of view.

Table 1. Analysis of input and output frequency according to internal sub module structure (unit: GHz)

Input freq.	Internal sub-band	Direct or converter	LO	Output freq.
0.5–2	0.5–2	Direct	No need	0.5–2
2–18	2–6	Direct	No need	2–6
	6–10	Converter	Need (12)	2–6
	10–14	Converter	Need (16)	2–6
	14–18	Converter	Need (12)	2–6

istics is required for each sub-band frequency, the rejection value was designed to suppress spurious using a cavity filter with a suspended structure rather than a general inductor & capacitor (L/C) or coupled line type.

In this paper, the input ports are classified by frequency band—low-band (0.5–2 GHz), mid-band (2–6 GHz), high-band (6–18 GHz), and full-band (2–18 GHz)—so that only the relevant signals are collected. When 18 GHz was input, the design approach proposed in this paper was implemented so that the frequency conversion function (frequency mixer and LO unit) inside the module would be converted into the IF (0.5–6 GHz) and transmitted it to the signal processing unit. The contents proposed in this paper are as follows.

First, the frequency of the 0.5–18 GHz band received by the antenna through the free space medium was designed to ensure isolation between paths to avoid affecting paths other than the corresponding path.

Second, instead of implementing the LO signal generation methodology necessary to convert the high frequency of 6–18 GHz to the middle frequency of 2–6 GHz, which would use a phase locked voltage controlled oscillator (PLVCO) for each of the three sub-bands, the system provides 1 GHz externally. The complexity of the circuit was simplified and the interference of signals was eliminated in advance through a design that enabled the reference frequency to be received and implemented in the form of multiplication.

Third, to reduce the mixed product components generated during frequency conversion, the out-of-band suppression characteristics of the band pass filter were improved, and an appropriate filter pass frequency was determined through spurious analysis. In addition, to suppress the original signal after multiplication of the LO path, cross-coupled band pass filters were applied by patterning the PCB.

Fourth, as several sub-modules must be connected with RF cables in the device, the structure was designed from a disassembly/assembly point of view for performance improvement (debugging) after assembly.

II. Wideband Frequency Down-Converter Structure

In this study, a down-converter module that can receive 0.5–18 GHz was mounted on the front end of the rear end of the antenna, with 6 RF inputs (0.5–2 GHz, 6–18 GHz, 2–18 GHz) and 1 IF output (0.5–6 GHz) and BIT input (0.5–18 GHz) ports. A limiter was applied in the first stage to protect internal components in the case that instantaneous over-input power was received, which also ensured an excellent noise figure. In addition, a high-pass filter was applied to remove unwanted low-band frequency components for each path.

Fig. 3 presents detailed configuration diagrams of the RF and LO sections of the multi-channel matrix and down-converter required for the ESM system. The frequency out of the 0.5–18 GHz signals received from the antenna without going through a frequency converter (mixer) is up to 0.5–6 GHz. By selecting the switch of the output stage (red circle), it is directly transferred to the IF output port, and the 6–18 GHz input frequency is inputted to the frequency converter via a filter bank to be down converted to the IF signal.

The required local oscillator signal was designed to receive an external reference frequency of 1 GHz from the system, multiply it by four, and then go through three additional multiplication paths to generate 12 GHz and four additional multiplication paths to generate another 16 GHz. The two paths were selected through a switch at the final stage, and each path is designed/applied by PCB patterning the band pass filter to

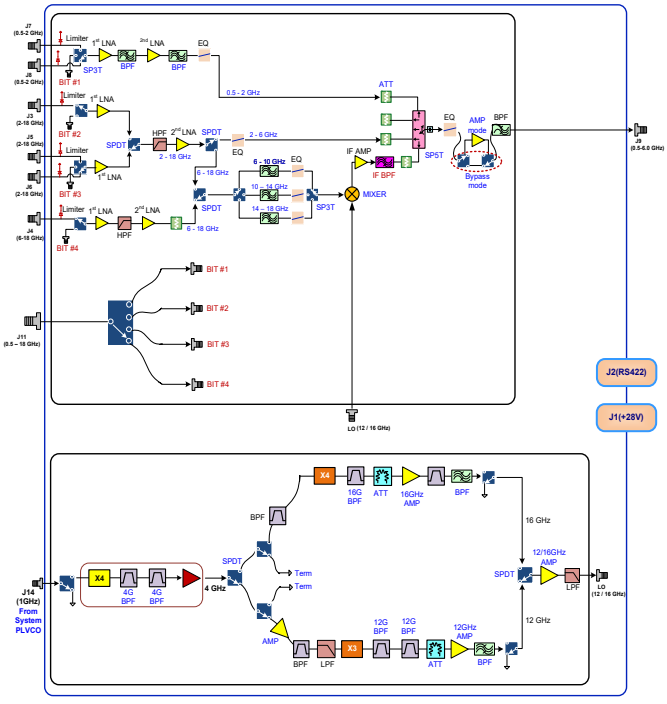


Fig. 3. Block diagram of frequency down converter module.

remove harmonic components generated at the rear end of multiplication and pass only the corresponding multiplication frequency.

III. Design and Simulation

1. Calculation of Frequency Plan for LO Path and Analysis of Mixed Product for IF Path

In the 6-18 GHz path that requires frequency conversion, the complexity of the LO circuit can be reduced through the method of implementing the LO frequency, thereby reducing unnecessary signals. Accordingly, when implemented in a simple form, as shown in Table 2, three LO frequencies are required, but the LO frequency is allocated to the lower sideband (LSB) instead of only the upper sideband (USB). It may be possible to design the circuit simply so that it can be implemented with only two frequencies. In addition, as the possibility of crosstalk through free space can be reduced by as much as the LO frequency is reduced, there is an advantage in excluding mixed spurious that may occur in the IF frequency band.

The frequency-specific images in Fig. 4 show the IF output frequency (2–6 GHz) for each RF path; these frequencies were used to attempt to predict in advance any unwanted product components that may be present in the IF frequency band of mixed product components generated in the frequency converter. These unnecessary components cannot be completely removed, and, as a result, the signal processing module must process the signal so that it is not affected by software. The expected spurious frequencies in the IF band are shown in Table 3.

2. Phase Noise Analysis for LO Section

The PLVCO method and the comb generator method can be used to implement a phase locked loop (PLL) LO that is phase-synchronized to an external reference frequency of 1 GHz; however, the PLVCO uses a it operates the complex, PLL integrated circuit (IC) that require the design of a voltage

Table 2. Frequency plan of LO frequency (unit: GHz)

	RF		Local freq.	IF	
	Low	High		Low	High
Three types of LO freq.	6	10	12	2	6
	10	14	16	2	6
	14	18	20	2	6
Three types of LO freq.	6	10	12	2	6
	10	14	16	2	6
	14	18	12	2	6

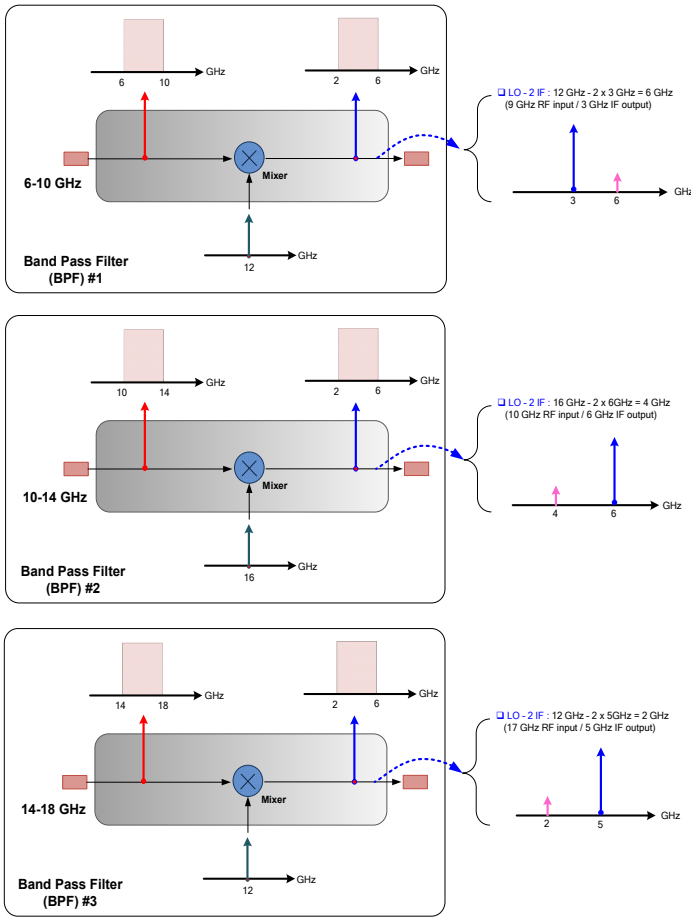


Fig. 4. Spurious analysis near the bandwidth of IF output frequency (2–6 GHz) for each RF path.

Table 3. Expected spurious frequencies near the bandwidth IF frequency (2–6 GHz) (unit: GHz)

RF		Local freq.	IF freq.	Spurious (LO-2IF)
Low	High			
6	10	12	2–6	2
10	14	16	2–6	4
14	18	12	2–6	8

controlled oscillator (VCO), PLLIC, and loop filter separately in each path, as shown in Fig. 5(a).

In this study, after 1 GHz was received and multiplied by four, the required 12 GHz and 16 GHz were generated through X3 and X4 in each path, as shown in Fig. 5(b). The phase noise of the *N*-multiplied frequency from the external reference will be deteriorated by as much as the multiplying factor as per Eq. (1) [6]:

$$Phase\ Noise = 20LOG10(N) \tag{1}$$

The results of phase noise analysis in the LO structure (comb generator, two paths) selected in this paper at 16 GHz, which is a high frequency path are shown in Table 4. Table 4 shows the

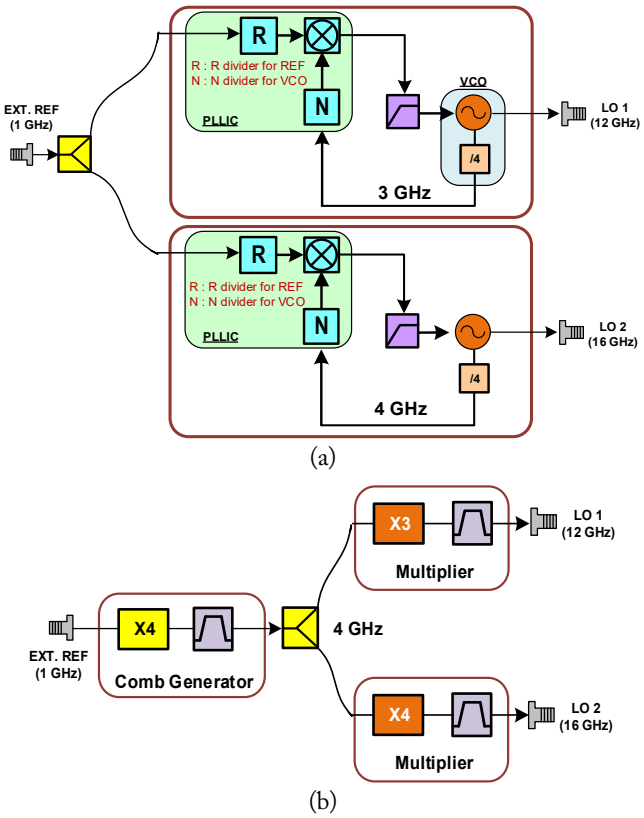


Fig. 5. (a) PLVCO with a complex circuit. (b) Comb generator with a simple circuit.

Table 4. Analyzed values of PN for the comb generator method (unit: dBc/Hz)

	Offset frequency				
	100 Hz	1 kHz	10 kHz	100 kHz	1 MHz
External ref. PN	−100	−130	−140	−155	−160
PN @ 12 GHz LO	−78	−108	−118	−133	−138
PN @ 16 GHz LO	−76	−106	−116	−131	−136

PN = phase noise.

analyzed values of phase noise for the 16 GHz LO path based on the comb generator method, which were −116 dBc/Hz at 10 kHz offset and -131 dBc/Hz at 100 kHz offset.

3. Filter Design with 16 GHz for LO Section

Regarding the LO implementation method applied in Section III-2, to pass the 16 GHz frequency generated after multiplying the comb generator output of 4 GHz, the pass band is designed to be a very narrow and, efficient cross-coupled band pass filters for suppressing adjacent frequencies.

We propose the use of the schematic shown in Fig. 6. The couplings between resonators 1 and 2 and between 3 and 4 were realized as mixed couplings (combination electric and magnetic),

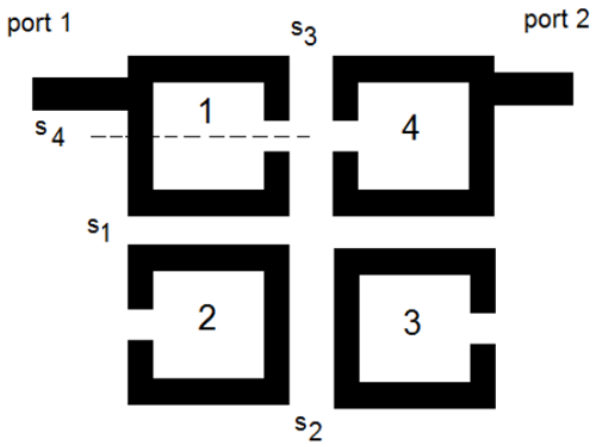


Fig. 6. Schematic for realizing the coupling.

whereas the coupling between resonators 2 and 3 was magnetically and that between 1 and 4 was electrical (negative coupling value). The couplings between resonators 1 and 2, 2 and 3, and 3 and 4 were the direct couplings, whereas the coupling between resonators 1 and 4 was a cross coupling, which realizes a transmission of zeros [7].

Fig. 7(a) and 7(b) show the PCB artwork and a graph of the simulation graph for the 16 GHz LO path. As a result of the simulation shown in Fig. 7(b), the insertion loss is 2.0 dB at 16 GHz, and the return loss is 20 dB or less (S_{11}: red color).

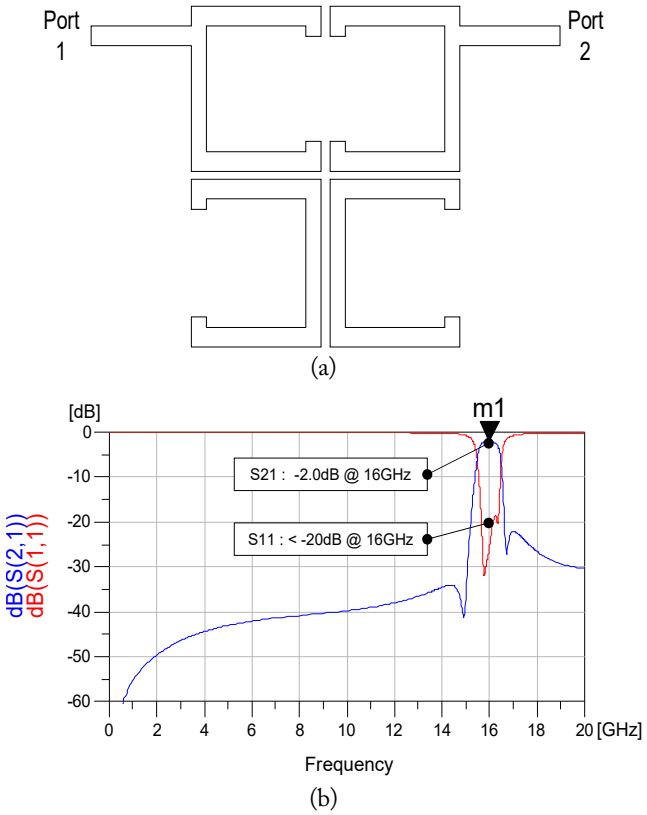


Fig. 7. (a) PCB artwork for realizing the coupling. (b) Simulation results for cross-coupled band pass filters.

4. Design of Broadband Bias Tee for RF Section

In the 2–18 GHz RF path, excluding the low band input (0.5–2 GHz) port, a broadband switch must be used to select the antenna port and the built-in test (BIT) port. The first switch should be designed to minimize loss so as not to affect noise or break impedance matching, for instance by producing resonance within a broadband frequency. When supplying the control signal necessary for the operation of the switch to each path, the inductor must select a component with an infinite value within the frequency.

Fig. 8(a) presents a circuit diagram of application schematic provided by the manufacturer showing and shows how the peripheral circuit of the broadband switch should be implemented [8]. Fig. 8(b) and 8(c) present a photo and graph of an evaluation JIG with a high inductance value (1.65 uH @ 10 MHz), which was manufactured by PICON-ICS Inc. Its measurement result was designed to use a switch and inductor that operate infinitely within the frequency band. The measured data shows the insertion loss for the operating path (frequency, 2–18 GHz) with a loss of −1.1 dB min in the first −2.3 dB max in the edge, including losses for the micro strip line and subminiature version-A (SMA) connector.

5. Analysis of Output Third Order Intercept Point (OIP3) for Each Path

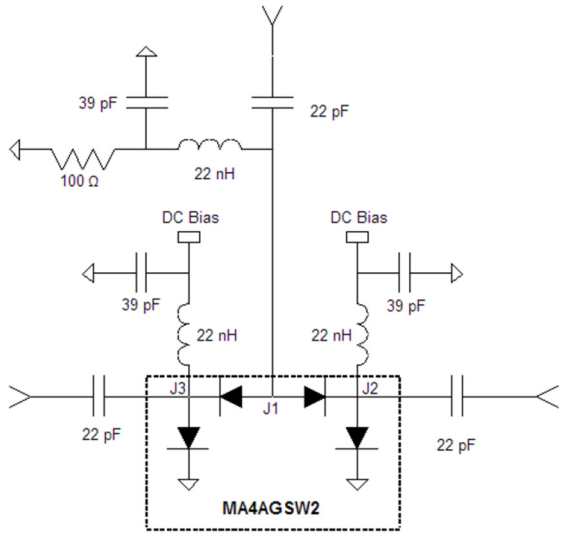
A broadband receiver module is vital to maintaining line-arity without distortion and is defined as an OIP3. To ensure a good performance by OIP3, it should be analyzed using a budget analysis tool to identify its limitations. Typically, Gain and OIP3 represent trade-offs because they prevent two items from obtaining a good performance at the same time. Additionally, the characteristics of OIP3 are important because they affect the signal quality of an analog-to-digital (AD) converter.

Fig. 9 shows the contents with a cascade path for each paths such a 0.5–2 GHz path (J7), a 2–6 GHz path (J3), and a 6–18 GHz path (J4). The expected results of each path are shown in Table 5.

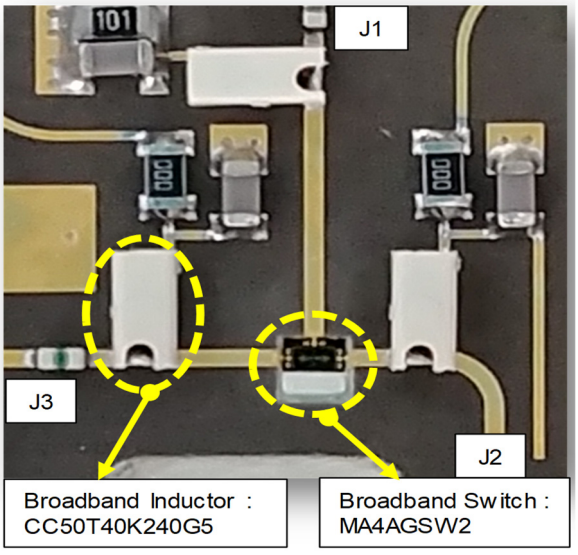
IV. Fabrication and Measurement

A broadband receiver module with six RF input ports (0.5–18 GHz), one IF output port (0.5–6 GHz), and 1 GHz reference port was designed so that the RF and LO regions were first physically separated. Sub-module units were assembled in each area, and each sub-module was assembled using bare MMIC and Rogers RT/duroid 5880 (0.127 mm) PCB to achieve downsizing and weight reduction.

A gallium arsenide (GaAs) MMIC chip was mounted on a gold-plated substrate to provide good grounding. A high-frequency PCB was placed around the chip to connect the DC



(a)



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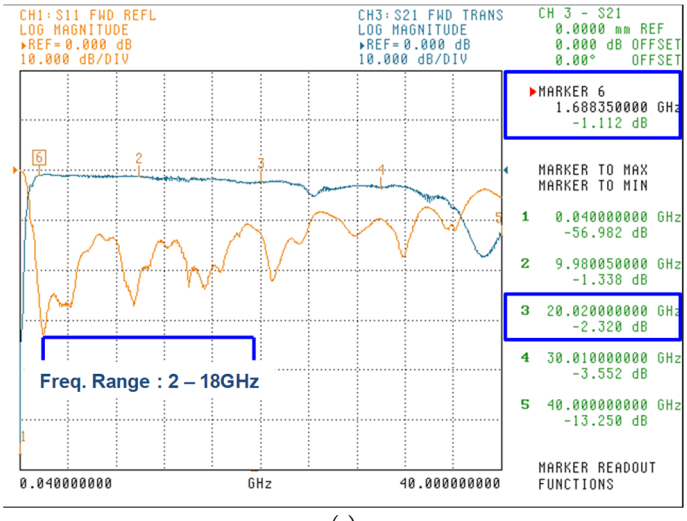


(c)

Fig. 8. (a) Schematic for bias tee circuit of switch. Adapted from [8]. (b) Photo of bias tee circuit of evaluation JIG. (c) Measured results for bias tee circuit of evaluation.

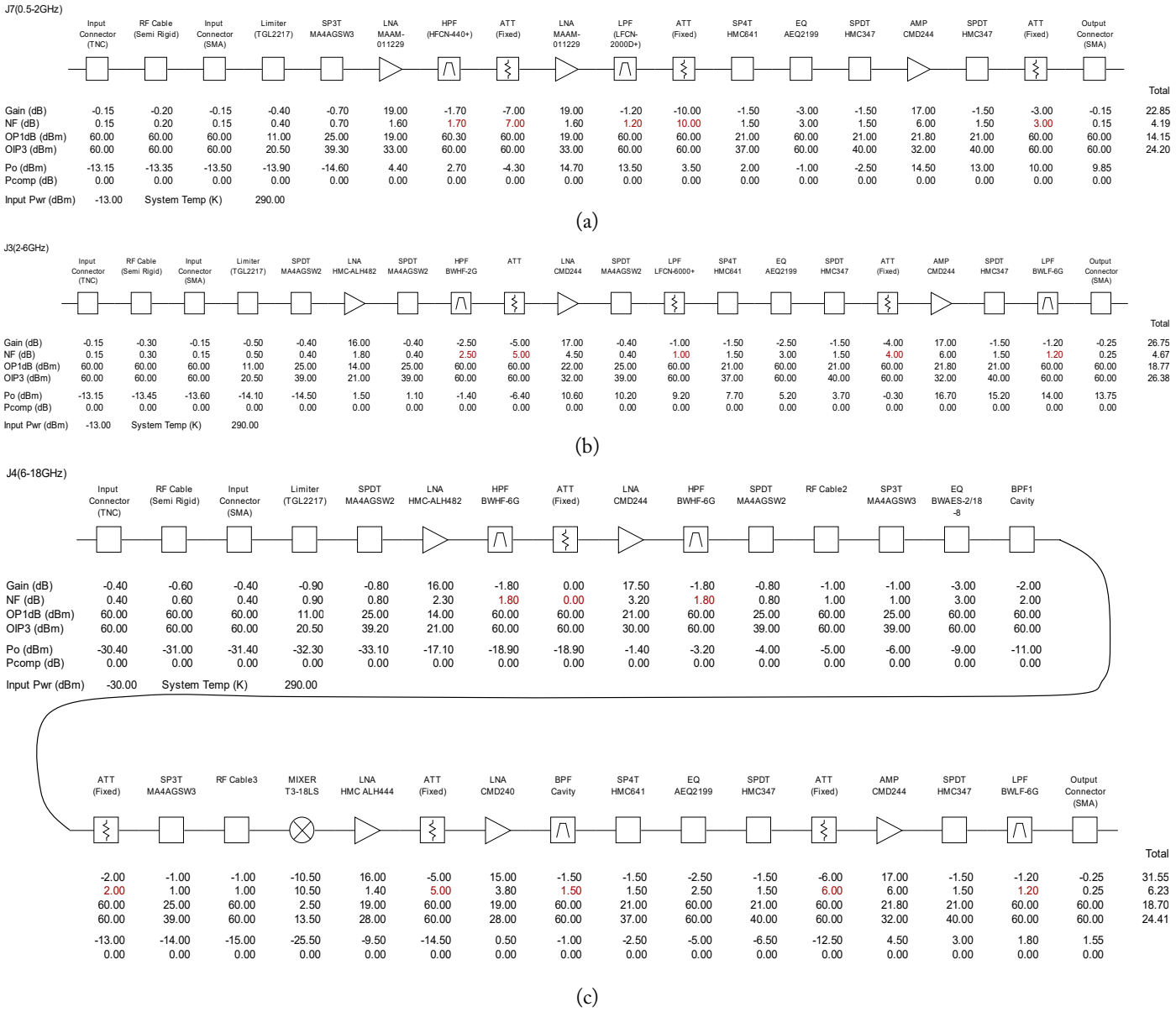


Fig. 9. Budget analysis to determine OIP3 value for each path: (a) 0.5–2 GHz path (J7), (b) 2–6 GHz path (J3), and (c) 6–18 GHz path (J4).

Table 5. Summarized values of OIP3 for each frequency band

Port	Freq. band (GHz)	Gain (dB)	OIP3 (dBm)
J7	0.5–2	22.85	+24.20
J3	2–6	26.75	+26.38
J4	6–18	31.55	+24.41

bias, and the input and output lines were wire bonded through a chip-and-wire process [9].

The frequency of the 0.5–18 GHz band was transferred through the transmission line to ensure the signal was transmitted without loss or distortion. In addition, to overcome the low frequency and narrow bandwidth limitations of existing products, bare-type MMIC devices with high operating frequencies and wide bandwidths instead of general package components were used to directly mount components to the housing. The chip-and-wire process was applied to minimize the mismatch [10].

Fig. 10 shows the assembled image of the whole box with four sub-modules (input, output, three channel filter bank, LO), control board, and RF semi-rigid cable. It can be seen that many cables are needed to connect the ports of the inner sub-module to the interface of the outer side. Fig. 11 shows the assembly procedure of the sub-module in the form of an illustration, and Fig. 12 shows a photo of a manufactured module with four sub-modules using bare type MMIC.

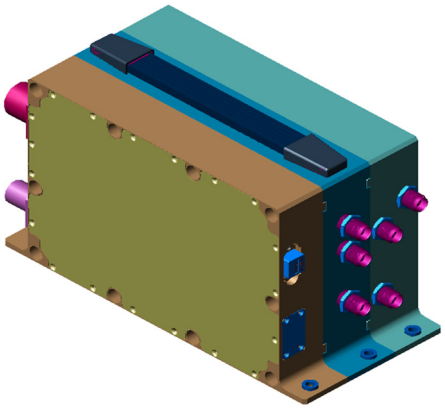


Fig. 10. Image of wideband frequency down converter module.

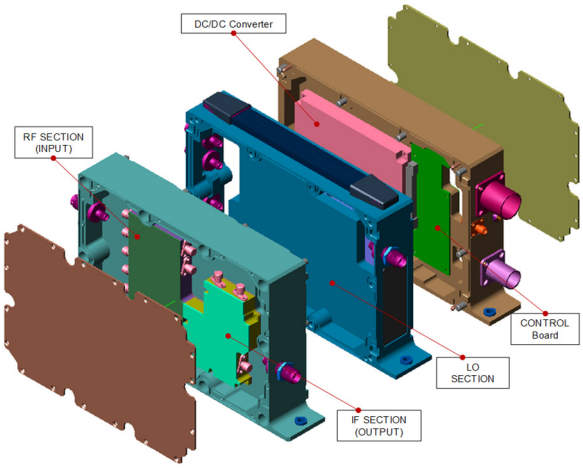


Fig. 11. An image of the integration process of wideband frequency down converter module (0.5–18 GHz).

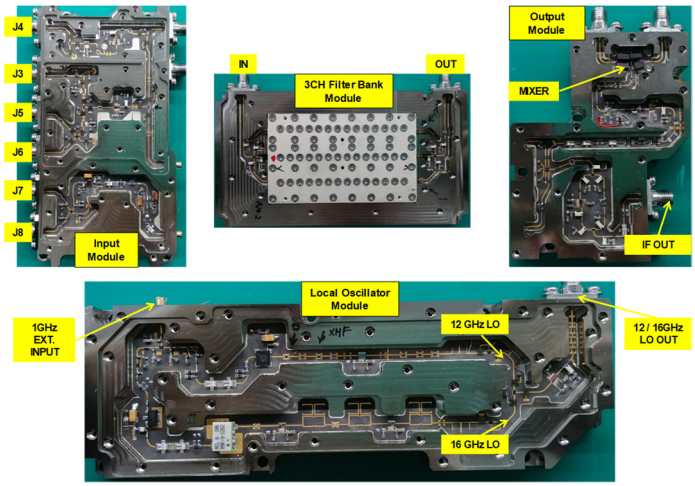
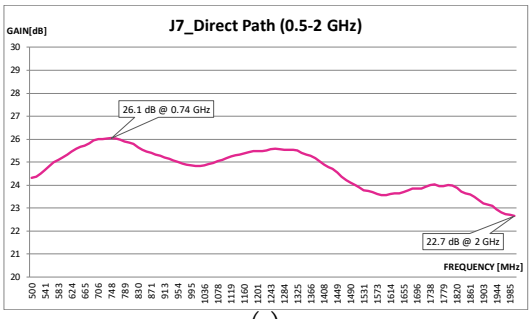


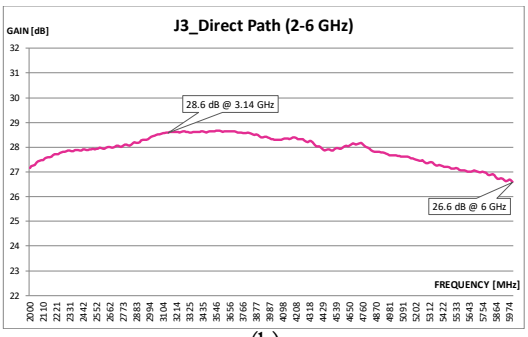
Fig. 12. Real picture of wideband frequency down converter module (0.5–18 GHz).

1. GAIN Measurement Results

Fig. 13(a) shows the gain graph for the RF input port (J7, frequency 0.5–2 GHz, direct path) with a gain of at least 22.7 dB in the band and a gain flatness of 3.4 dB at maximum. Fig.



(a)



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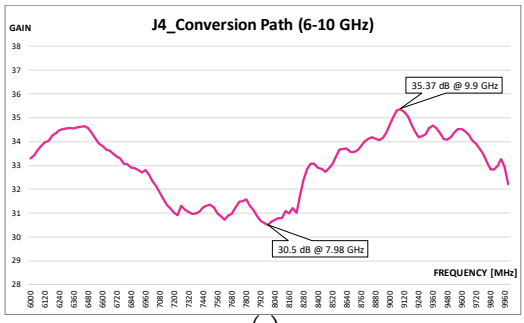

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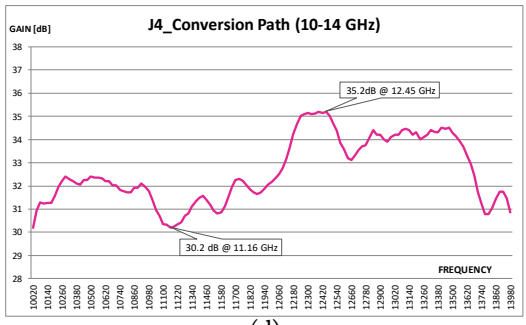

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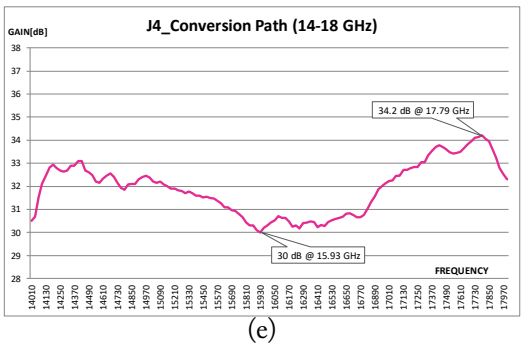


(e)

Fig. 13. Results of RF input port: (a) J7 port (0.5–2 GHz), (b) J3 port (2–6 GHz), (c) J4 port (6–10 GHz), (d) J4 port (10–14 GHz), and (e) J4 port (14–18 GHz).

13(b) shows the gain graph for the RF input port (J3, frequency 2–6 GHz, direct path) with a gain of at least 26.6 dB in the band and a gain flatness of 2.0 dB at maximum. Fig. 13(c) shows the gain graph for the RF input port (J4, frequency 6–10 GHz, converter path) with a gain of at least 30.5 dB in the band and a gain flatness of 4.87 dB at maximum. Fig. 13(d) shows the gain graph for the RF input port (J4, frequency 10–14 GHz, converter path) with a gain of at least 30.2 dB in the band and a gain flatness of 5.0 dB at maximum. Fig. 13(e) shows the gain graph for the RF input port (J4, frequency 14–18 GHz, converter path) with a gain of at least 30.0 dB in the band and a gain flatness of 4.2 dB at maximum.

The measured gain value is almost the same as the minimum gain value for each band required at the system level, as shown in Fig. 2; this demonstrates that it can be installed in a real system and operate without problems. In addition, the higher the frequency, the higher the gain value was set to compensate for the gain reduction of other devices (especially the RF cable). The measured results of each path are shown in Table 6.

2. Spurious (LO-2IF) Measurement Results

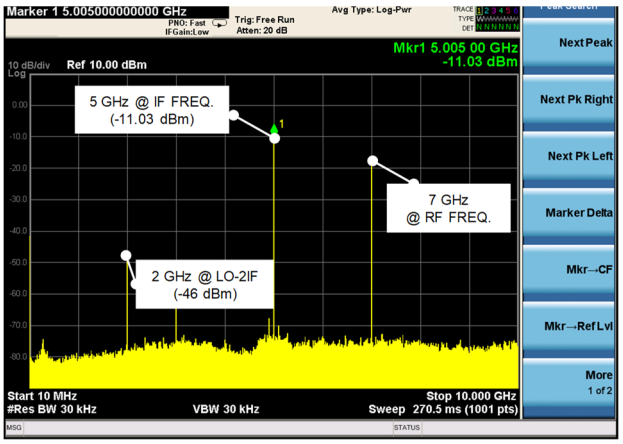
The measured results of each path are shown in Table 7 and were the same as with spurious frequency, based on the predictions presented in Fig. 4. These values shown in Fig. 14 cannot be deleted from the output port because they are in the band. Therefore, the signal process should account for these spurious frequencies when processing at the system level.

Table 6. Summarized values of the main items for each frequency band

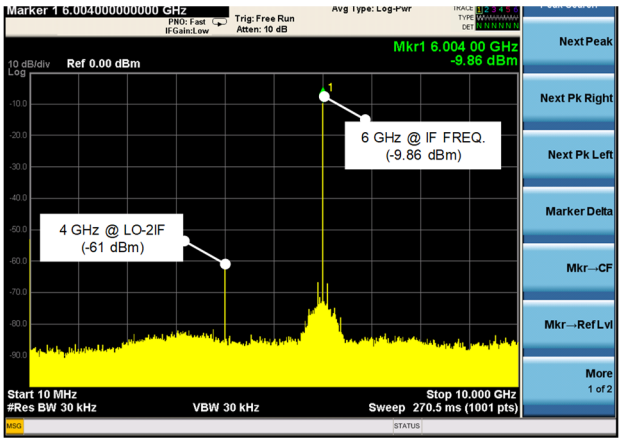
	Gain (dB)	
	Expected	Measured
J7 (0.5–2 GHz)	22.0	22.7
J3 (2–6 GHz)	26.0	26.6
J4 (6–10 GHz)	30.0	30.5
J4 (10–14 GHz)	30.0	30.2
J4 (14–18 GHz)	30.0	30.0

Table 7. Summarized values of the spurious delta for 6-18 GHz frequency

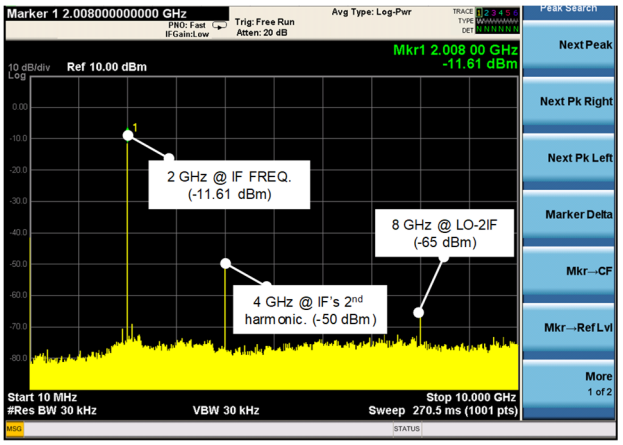
RF (GHz)		Spurious freq. (GHz)	Measured value (dBc)
Input freq.	Output freq.		
6–10	5	2	34.97
10–14	6	4	51.14
14–18	2	8	53.39



(a)



(b)



(c)

Fig. 14. Measurements of spurious for each path: (a) BPF1 (6–10 GHz), (b) BPF2 (10–14 GHz), and (c) BPF3 (14–18 GHz).

3. Output Third Order Intercept Point (OIP3) Measurement Results

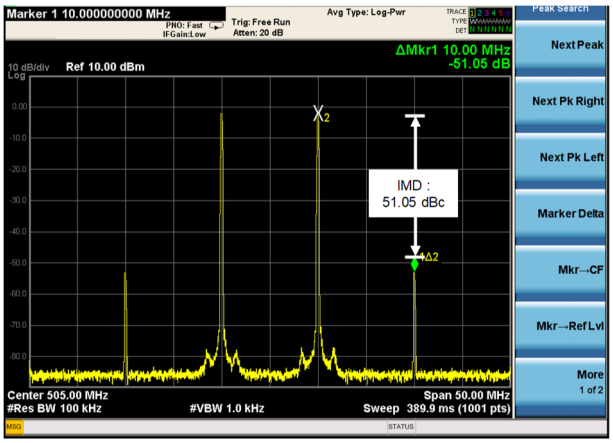
The OIP3 from the measured intermodulation distortion (IMD) will be calculated by as per Eq. (2) [11]:

$$OIP3 = \text{Output Power} + \frac{IMD}{2} \ (dBm) \quad (2)$$

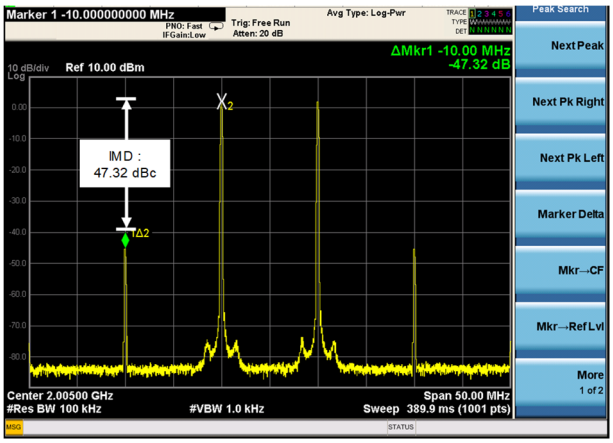
The measured results of each path are shown in Table 8 and Fig. 15.

Table 8. Calculated values of OIP3 for each frequency band

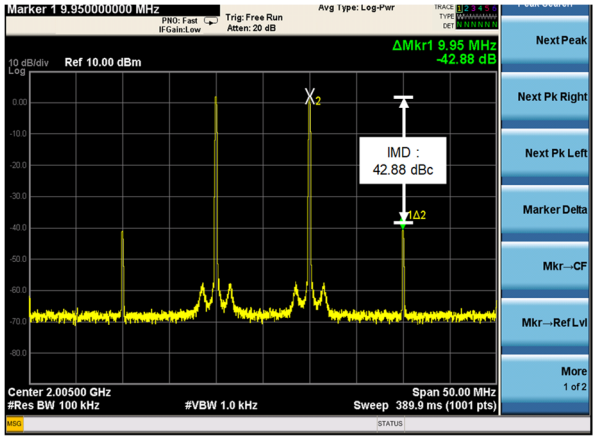
Port	Freq. band (GHz)	Output power (dBm)	IMD (dBc)	OIP3 (dBm)
J7	0.5–2	−2.0	51.05	+23.52
J3	2–6	+2.0	47.32	+25.66
J4	6–18	+2.0	42.88	+23.44



(a)



(b)



(c)

Fig. 15. Measurements of IMD at each port: (a) J7 port, (b) J3 port, and (c) J4 port.

OIP3 values, which were analyzed in Section III-5 were slightly lower than the measured data. However, these values can be considered reasonable because there are many unknown factors in practice, such as the lower linearity of the amplifier, mismatching among components, and assembly conditions of soft material PCB.

V. Conclusion

In this paper, we used a bare-type MMIC device and applied a chip-and-wire process to design and fabricate a wideband frequency down converter module with a local circuit with high gain, low spurious, high IP3 characteristics, and reliability. To compensate for the mismatch among many sub-modules, we designed an input module, filter bank module, output module, and local oscillator module suitable for sub-band frequency characteristics and applied them to the down converter. The down converter module has three paths, which were divided for 0.5–2 GHz (direct), 2–6 GHz (direct), and 6–18 GHz (converter). Amplitude-matched RF semi-rigid cables of different lengths were used to connect to the internal sub-modules of the frequency down converter. The main RF line was a dielectric substrate (RT/duroid 5880) with a relative dielectric constant of 2.2 and a dielectric thickness of 0.127 mm.

The gain obtained at low-band was 22.7 dB (input frequency 0.5–2 GHz), and the flatness was about 3.4 dB. The gain was 26.6 dB at mid-band (input frequency 2–6 GHz) and the flatness was about 2.0 dB. The gain in high-band (input frequency 6–18 GHz) was 30.5 dB at 6–10 GHz, 30.2 dB at 10–14 GHz, 30.0 dB at 14–18 GHz.

The measured values of IP3 were +23.52 dBm, +25.66 dBm and +23.44 dBm as the maximum value. The measured value of spurious (LO-2IF) at the converter path was 34.97 dBc as the maximum value. The proposed 0.5–18 GHz wideband frequency down converter module can be applied to a front-end amplifier that requires path selection at the back of the antenna of an ESM system.

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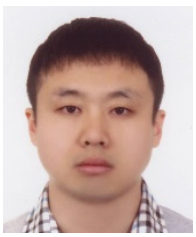

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