CMOS Wideband Low-Pass Filter Using Complementary Structured OPAMP for Wideband System Applications

Chang-Kyun Noh · Hyun-Yeop Lee · Ho-Jin Kang · Seong-Tae Kim · Ho-Seon Baek · Young-Jin Kim[*]

Abstract

In this paper, a CMOS wideband low-pass filter is proposed. In the wide band active filter design, the unit gain frequency (GBW) of OPAMP should be larger than GHz. The GBW of the proposed OPAMP is around 2.3 GHz. Additionally, the OPAMP with a complementary structure in signal and common mode feedback is proposed and has a wide operating voltage range at the input and output. The 1-dB gain compression point (P1dB) at the output is 4.9 dBm. A source follower is employed for driving 50 Ω output impedance without degrading the bandwidth and linearity of the filter. The power consumption is 27 mW from a 1-V supply voltage. The 3 dB bandwidth of the filter ranges from 330 MHz to 660 MHz with 3-bit cap tuning. This work is implemented in a 65-nm CMOS process, with a chip area of 0.18 mm².

Key Words: Active RC Filter, Analog Filter, Low-Pass, Common Mode Feedback (CMFB), OPAMP.

I. INTRODUCTION

In recent years, the Internet of Things, autonomous driving, and artificial intelligence based on 5G have emerged as interesting new trends. By following these trends, 3GPP recently published a Release-17 about 5G communication protocols, which includes information about frequency usage standards [1]. In the new standard, there are two main features that rely on dual band modulation and multiple antennas for multiple-input multiple-output (MIMO) in higher and wider frequency bands than previous protocols. As a result, a faster data rate and lower latency could be achieved. However, because of the high and wide operating frequency channel bandwidth, RFIC design specification would be more difficult. Fig. 1 shows the 5G fre-
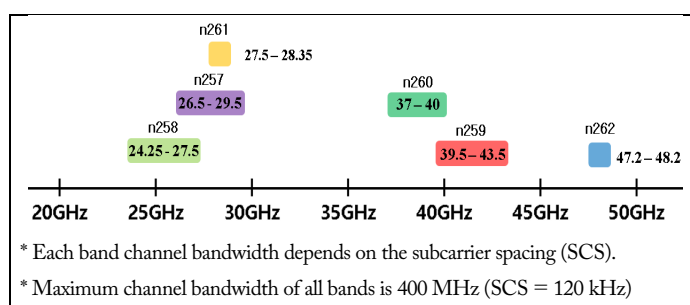

Fig. 1. A 5G FR2 band allocation.

quency FR2 band of which the maximum channel bandwidth is up to 400 MHz when subcarrier spacing (SCS) is 120 kHz. Designing for a higher frequency than the FR1 band, which can

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handle up to 6 GHz, is required. This implies that the receiver should cover a wider bandwidth, which would have a greater number of adjacent channel interferences and unwanted signals in the high frequency band than prior models. To achieve these requirements, it is necessary to have high filter rejection at a higher cutoff frequency than that of conventional low-pass filters (LPFs) of several megahertz.

Tables 1 and 2 represent the adjacent channel selectivity (ACS) requirements and its test parameters, based on QPSK modulation in the 5G OFDM-TDD (orthogonal frequency division multiplexing-time division duplex) system. The requirement is a minimum of 22 dB in all channel bandwidths for over 95% throughput when the maximum power of the interfere signal near the wanted signal is −25 dBm. In the receiver chain, this ACS is usually achieved by a high-order LPF design in the baseband. Because of the emerging 5G standard, and previous research (e.g., [2]) not covering bandwidth and rejection level, this paper proposes a wideband fourth order LPF, which is a part of the transceiver, using complementary structure OPAMP. The advantages and design principles of complementary structure will be described in Section II. Section III presents the simulation and measurement results, and Section IV concludes this work.

Table 1. A 5G NR band adjacent channel selectivity (unit: dB)

Operating band	Adjacent channel selectivity/channel bandwidth			
	50 MHz	100 MHz	200 MHz	400 MHz
n257, n258, n261	23	23	23	23
n259, n260, n262	22	22	22	22

NR = new radio.

Table 2. Adjacent channel selectivity test parameters

Operating band	Adjacent channel selectivity/channel bandwidth			
	50 MHz	100 MHz	200 MHz	400 MHz
Subcarrier spacing (kHz)	120	120	120	120
Modulation	QPSK	QPSK	QPSK	QPSK
Max throughput, 1 frame (Mbps)	10.02	20.28	40.59	81.101
Signal power (dBm)	−46.5	−46.5	−46.5	−46.5
Interfere power (dBm)	-25	-25	-25	-25
Interfere BW (MHz)	50	100	200	400

II. A Fourth Biquadratic Filter Design

The fourth-order LPF is shown in Fig. 2. It consists of two biquadratic filters and a complementary, structured source follower (SF). Because the active R-C filter is sensitive to low load impedance, the SF drives at the final stage for interfacing external instruments. If low load impedance is connected in the next stage without SF, the quality factor (Q-factor) of LPF is degraded by low load impedance.

1. Biquadratic Filter

In LPF design, if the GBW of OPAMP is the same as or larger than the LPF's 3 dB frequency, the changes in the characteristics of the LPF by OPAMP can be ignored. At the same time, in wideband LPF, because the pole of OPAMP may not cover the LPF's 3 dB frequency, exact calculation with non-ideal OPAMP should be considered. Figs. 3 and 4 show the biquad-
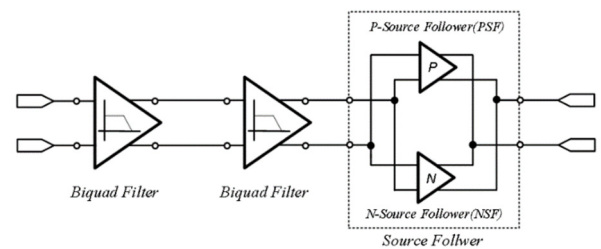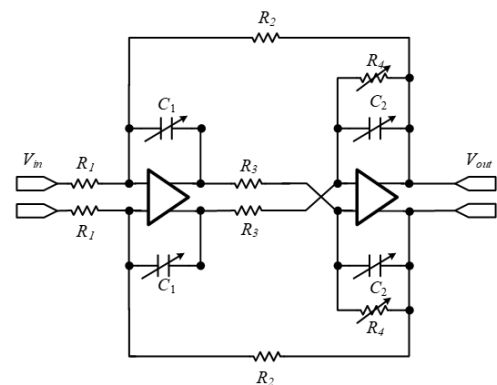

Fig. 2. Overall block diagram.

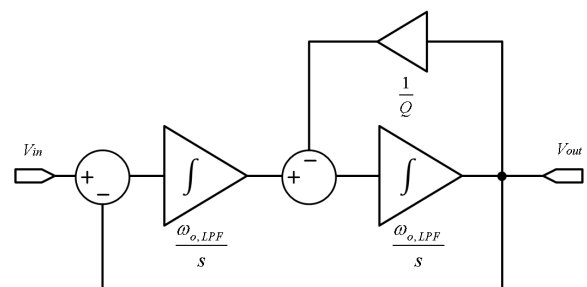Fig. 3. Biquadratic filter with non-ideal OPAMP.

Fig. 4. Biquadratic filter's system block diagram.

ratic filter circuit with OPAMP and a system block diagram. The filter is equal to a feedback circuit with $1/Q$ and unit gain feedback paths and two integrators. The transfer function of the block diagram is expressed in Eq. (1). In Fig. 4, because OPAMP should operate as an integrator to be the same as the ideal transfer function, OPAMP performance is crucial. In the conventional integrator, which is shown in Fig. 5, OPAMP is not ideal, and its transfer functions should be calculated to equal the ideal transfer function. Eq. (2) shows the calculations of the integrator transfer function with a single pole OPAMP system. This means that if the pole of the OPAMP system is the same as the integrator's 3 dB frequency, and gain is sufficient for a feedback loop, the integrator transfer function can neglect the OPAMP's non-ideality. Fig. 6 shows the calculation of the transfer function with a non-ideal OPAMP. It should be assumed that the required minimum gain in an open loop system to obtain a closed loop gain is 40 dB, and OPAMP variables of 3 dB frequency make the filter transfer function change. To be the same as the ideal transfer function, the figure shows that the OPAMP's frequency should be at least 0.1 times the filter transfer function. Fig. 7 represents each Q-factor of the biquadratic filter. The proposed filter follows the response of the worth filter.
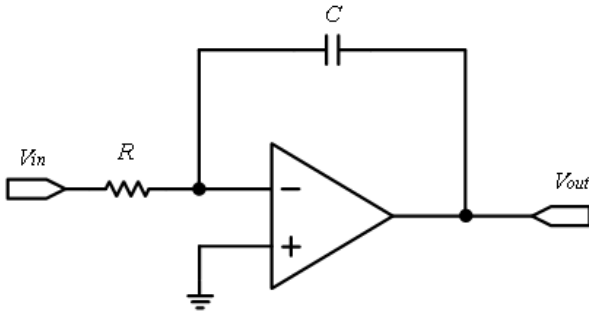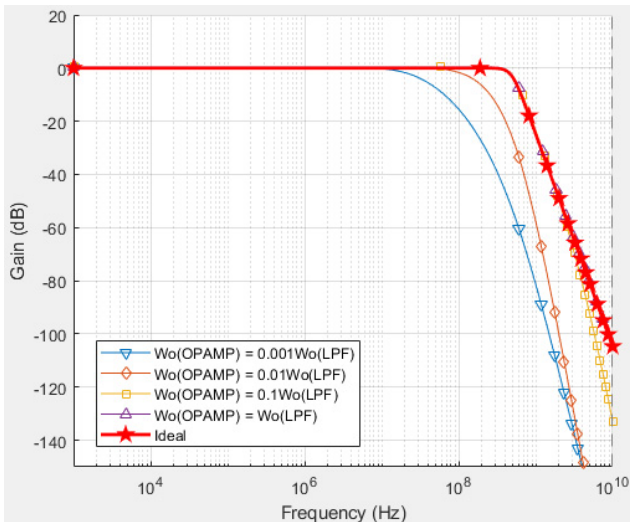

Fig. 5. Conventional integrator.

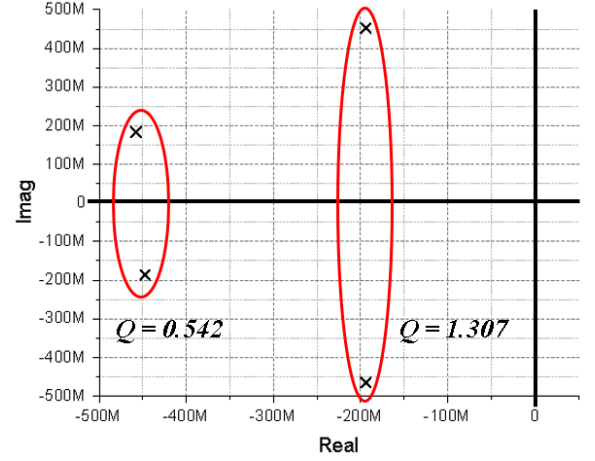Fig. 6. Transfer function with non-ideal OPAMP of 3 dB frequency variation ($A_{o,amp} = 40$ dB).

Fig. 7. The fourth order filter transfer function pole and zero plot.

$$H(s)_{Biquad} = \left| \frac{V_{out}}{V_{in}} \right| = \left| \frac{-\dfrac{1}{C_1 C_2 R_1 R_3}}{s^2 + \dfrac{s}{C_2 R_4} + \dfrac{1}{C_1 C_2 R_2 R_3}} \right|$$

$$= \frac{\dfrac{1}{C^2 R^2}}{s^2 + \dfrac{s}{C R_4} + \dfrac{1}{C^2 R^2}}$$

$$= \frac{\omega_{o,LPF}^2}{s^2 + s\left(\dfrac{\omega_{o,LPF}}{Q}\right) + \omega_{o,LPF}^2} \quad ,$$

$$\left(\omega_{o,LPF} = \frac{1}{CR}, Q = \frac{R_4}{R}\right) \qquad (1)$$

$$H(s)_{integrator} =$$
$$\frac{-A_o \omega_{o,amp}}{(s + \omega_{o,amp})sCR + sCRA_o\omega_{o,amp} + s + \omega_{o,amp}}$$
$$\approx \frac{-A_o \omega_{o,amp}}{(sCR + 1)(s + A_o\omega_{o,amp})} \approx \frac{-\omega_{GBW,amp}}{(sCR + 1)\omega_{GBW,amp}}$$
$$= \frac{-1}{sCR + 1}$$
$$(If \ \omega_{GBW,amp} = A_o\omega_{o,amp} \gg \omega_{o,LPF} \& A_o \gg 100 =$$
$$40 \text{ dB}). \qquad (2)$$

2. Wide Unit Gain Frequency OPAMP

This brief section will describe the proposed OPAMP, which was designed in two stages. Fig. 8 represents the proposed OPAMP. In the receiver baseband part, the roles of the variable gain amplifier (VGA) and LPF are amplifying the down-converted signals and filtering unwanted signals [3]. Thus, the linearity of the baseband is crucial. This means that the LPF should drive large input and output signals without gain compression. However, an NMOS single input cannot drive a signal near the ground, and PMOS cannot drive near the supply. This means the single MOS type of OPAMP suffers gain compression from the triode region near the supply or ground. Meanwhile, a complementary structure ensures the operation of saturation mode within a wider input/output range than the single
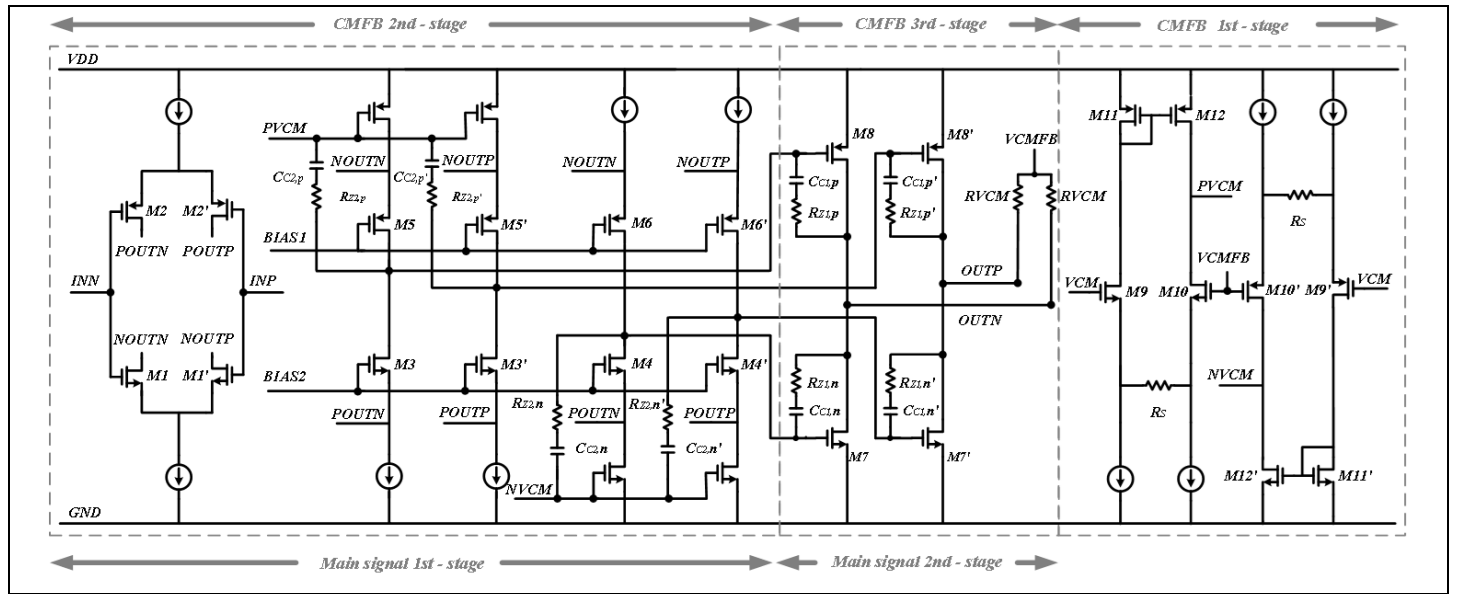
Fig. 8. OPAMP overall schematic.

MOS type. The complementary structure has nearly twice the transconductance of the single MOS type, with the added advantage of a larger GBW. For understanding the complementary structure, compare with previous studies [4–8]. As a result, complementary is appropriate when designing an LPF. The proposed OPAMP consists of the main signal part and the common mode feedback (CMFB) part, the structures of which are complementary. The main signal part is divided into two stages and the CMFB part is in three stages.

2.1. Main signal part

The main signal part is shown in Fig. 8. The main signal part has a PMOS and NMOS complementary structure. This structure can achieve larger transconductance, because the PMOS and NMOS of the input stage operates simultaneously. The proposed OPAMP consists of two complementary two stages, which are the folded cascode stage and common source stage. For stability, the OPAMP should be designed with a single pole system. Because of the two stages, as the result, the Miller compensation technique is used [9]. The folded cascode stage has two poles, and the common source stage has one pole. However, because one pole of the folded cascode is usually out of the GBW, only one Miller compensation is needed in the circuit. As a result, the transfer function and pole-zero calculation in the main signal part are calculated as shown in Eq. (3). If satisfying the condition in Eq. (4), the transfer function is approximately a single pole system.

$$A_v = \frac{A_{v,DC}\left(1 - \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)\left(1 + \frac{s}{\omega_{p3}}\right)} \tag{3}$$

$$\approx \frac{A_{v,DC}}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p3}}\right)} \approx \frac{A_{v,DC}}{\left(1 + \frac{s}{\omega_{p1}}\right)}$$

$$\because \omega_{p2} \approx \omega_z, \qquad \omega_{GBW} << \omega_{p3} \tag{4}$$

Fig. 9 shows the main signal part's small-signal equivalent circuits. The output of the first folded cascode stage is cascaded with the NMOS and PMOS inputs of the second common source stage. The exact pole-zero calculation is represented in Eqs. (5)–(6), where R_{n1}, R_{p1}, R_{n2}, R_{p2}, and C_{n1} to C_{n3} and C_{p1} to C_{p3} represent the resistances and capacitances of each stage, and $g_{mA,n}$ to $g_{mC,n}$ and $g_{mA,p}$ to $g_{mC,p}$ refer to transconductance, respectively as shown in Table 3.

$$\omega_{p1,n} = \frac{1}{R_{n1}\left(C_{n1} + g_{m2,n}R_{n2}C_{c,n}\right)},$$

$$\omega_{p2,n} = \frac{1}{R_{n2}(C_{n2}+C_{c,n})}, \ \omega_{p3,n} = \frac{1}{\frac{1}{g_{m3,n}}C_{n3}}$$

$$\omega_{z,n} = \frac{1}{C_{c,n}\left(\frac{1}{g_{m2,n}} - R_{z,n}\right)},$$

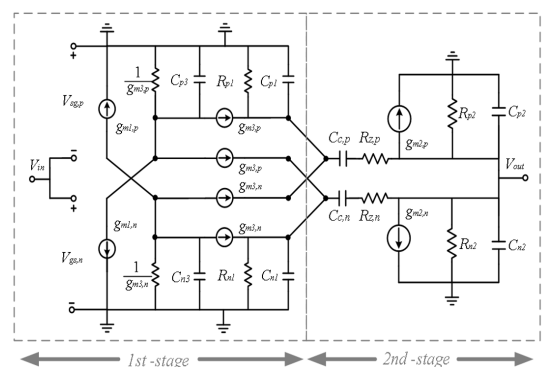$$A_{v,DC} = \left(g_{m1,n} + g_{m1,p}\right)R_{n1}g_{m2,n}R_{n2} \tag{5}$$

Fig. 9. Main signal part small signal equivalent circuit.

Table 3. OPAMP signal loop parameter

Parameter	Description		
R_{n1}	$(g_{m5}r_{o5})(r_{o1}\|r_{o13})\|r_{o3}$		
R_{p1}	$(g_{m4}r_{o4})(r_{o2}\|r_{o43})\|r_{o6}$		
$R_{n2} = R_{p2}$	$r_{o7}\|r_{o8}$		
C_{n1}	$C_{c2,n} + g_{m7}(r_{o7}\|r_{o8})C_{c1,n}$		
C_{p2}	$C_{c2,p} + g_{m8}(r_{o7}\|r_{o8})C_{c1,p}$		
C_{n2}	$C_{c1,n}$		
C_{p2}	$C_{c1,p}$		
C_{n3}	$C_{gs13}+C_{sb13} + C_{db5} + C_{gd5}+C_{db1}$		
C_{p3}	$C_{gs13}+C_{sb13} + C_{db5} + C_{gd5}+C_{db1}$		
$g_{mA,n}$	g_{m1}	$g_{mA,p}$	g_{m2}
$g_{mB,n}$	g_{m7}	$g_{mB,p}$	g_{m8}
$g_{mC,n}$	g_{m3}	$g_{mC,p}$	g_{m6}

$$\omega_{p1,n} = \frac{1}{R_{p1}\left(C_{p1} + g_{m2,p}R_{p2}C_{c,p}\right)},$$

$$\omega_{p2,n} = \frac{1}{R_{p2}\left(C_{p2} + C_{c,p}\right)}, \omega_{p3,n}\frac{1}{\frac{1}{g_{m3,p}}C_{p3}}$$

$$\omega_{z,n} = \frac{1}{C_{c,p}\left(\frac{1}{g_{m2,p}} - R_{z,p}\right)},$$

$$A_{v,DC} = (g_{m1,p} + g_{m1,n})R_{p1}g_{m2,p}R_{p2} \tag{6}$$

Each pole and zero approximation of the NMOS-path and PMOS-path is shown in Eqs. (7)–(8). The dominant pole of each path is the node of the middle of the first and second stages. Because of second stage gain, which is boosted by Miller capacitance in signal loop and Miller capacitance in CMFB loop, as well as LHP zero and pole cancellation, the second pole could be abbreviated without any effect. The third pole, which is larger than the GBW, is neglected. The total gain of OPAMP is the sum of the NMOS and PMOS pair, as shown in Eq. (9).

$$A_{v,n} \approx \left[\frac{(g_{m1,n} + g_{m1,p})R_{n1}}{\left(1 + sR_{n1}\left(C_{n1} + g_{m2,n}R_{n2}C_{c,n}\right)\right)}\right]g_{m2,n}R_{n2} \tag{7}$$

$$A_{v,p} \approx \left[\frac{(g_{m1,p} + g_{m1,n})R_{p1}}{\left(1 + s\left(C_{p1} + g_{m2,p}R_{p2}C_{c,p}\right)R_{p1}\right)}\right]g_{m2,p}R_{p2} \tag{8}$$

$$A_v = A_{v,n} + A_{v,p} \tag{9}$$

The total transfer function is shown in Eq. (10):

$$A_v = \left[\frac{(g_{m1,n} + g_{m1,p})R_{n1}}{\left(1 + s\left(C_{n1} + g_{m2,n}R_{n2}C_{c,n}\right)R_{n1}\right)}\right]g_{m2,n}R_{n2}$$

$$+ \left[\frac{(g_{m1,p} + g_{m1,n})R_{p1}}{\left(1 + s\left(C_{p1} + g_{m2,p}R_{p2}C_{c,p}\right)R_{p1}\right)}\right]g_{m2,p}R_{p2} \tag{10}$$

2.2. Common Mode Feedback Part

Regarding the LPF, the circuit is usually designed as a kind of feedback circuit that consists of a passive component and OPAMP. However, the feedback path does not contribute to the stability of the output node's DC level. The instability of the output node DC's level causes performance degradation. To prevent its saturation, a CMFB circuit should be considered to determine DC level in the OPAMP. The CMFB part is shown in Fig. 8. It consists of three stages: a current mirror load OTA, telescopic cascode, and common source stage. The main CMFB part is necessary to determine the output's common mode voltage. Thus, a low main dominant pole frequency does not cause any issues in the circuit. Because the three stages and two Miller compensations are used, there is a trade-off point between high DC gain and low dominant pole frequency.

Fig. 10 represents the small-signal equivalent circuit of the CMFB part, which is a complementary structure with the NMOS and PMOS pairs. Between each stage, Miller compensation is used. The CMFB loop should be a single pole system like the signal path, as shown in Eq. (11). At this point, the second zero is right-half-plane (RHP) zero, which decreases the phase by 90°. Thus, the third pole and second zero should be 10 times larger than the GBW frequency, as shown in Eq. (12).

The exact pole-zero calculation is represented in Eqs. (13)–(14), where $R_{L1,n}$ to $R_{L3,n}$ and $R_{L1,p}$ to $R_{L3,p}$ and $C_{L1,n}$ to $C_{L3,n}$ and $C_{L1,p}$ to $C_{L3,p}$ represent the resistances and capacitances of each stage, and g_{mnA} to g_{mnC}, and g_{mpA} to g_{mpC} indicate transconductance, respectively, and are shown in Table 4. The CMFB part is the same as the main signal part with the NMOS and PMOS pair, as shown in Eqs. (15)–(16). The total gain is the sum of the NMOS and PMOS pair, as shown in Eq. (17).

$$A_v = \frac{A_{v,DC}\left(1-\frac{s}{\omega_{z1}}\right)\left(1-\frac{s}{\omega_{z2}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)\left(1+\frac{s}{\omega_{p3}}\right)} \approx \frac{A_{v,DC}}{\left(1+\frac{s}{\omega_{p1}}\right)} \tag{11}$$
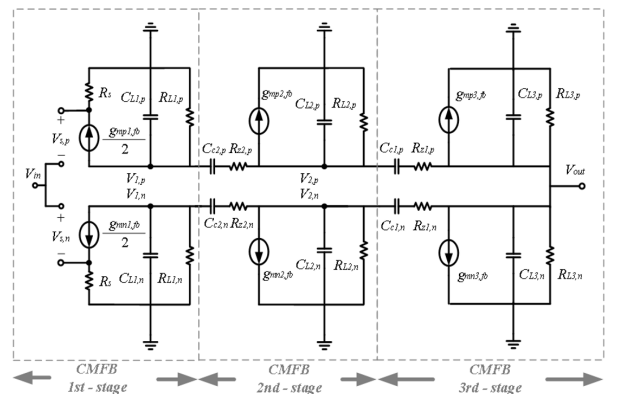

Fig. 10. CMFB part small signal equivalent circuit.

Table 4. OPAMP CMFB loop parameter

Parameter	Description
$R_{L1,n}$	$(g_{m10}r_{o10}R_s + R_s)\|r_{o12}$
$R_{L1,p}$	$(g_{m10'}r_{o10'}R_s + R_s)\|r_{o12'}$
$R_{L2,n}$	$(g_{m5}r_{o5}r_{o13}\|r_{o3})/2$
$R_{L2,p}$	$(g_{m4}r_{o4}r_{o15}\|r_{o6})/2$
$R_{L3,n} = R_{L3,p}$	$r_{o7}\|r_{o8}$
$C_{L1,n}$	$(g_{m13}(g_{m5}r_{o5}r_{o13}\|r_{o3})C_{c2,p})/2$
$C_{L1,p}$	$(g_{m14}(g_{m4}r_{o4}r_{o15}\|r_{o6})C_{c2,n})/2$
$C_{L2,n}$	$2(C_{c2,n} + g_{m7}(r_{o7}\|r_{o8}))C_{c1,n}$
$C_{L2,p}$	$2(C_{c2,p} + g_{m8}(r_{o7}\|r_{o8}))C_{c1,p}$
$C_{L3,n} = C_{L3,p}$	$C_{c2,n}$
$g_{mnA} = g_{mpA}$	g_{m10}
$g_{mnB} = g_{mpB}$	$g_{m14} + g_{m14'}$
$g_{mnC} = g_{mpC}$	$g_{m7} + g_{m7'}$

$$\because \omega_{p2} \approx \omega_{z1}, \omega_{p3} \gg \omega_{GBW}, \qquad \omega_{z2} \gg \omega_{GBW} \tag{12}$$

$$\omega_{p1,n} = \frac{1}{R_{L2,n}(C_{c1,n} + g_{mn3,fb}R_{L3,n}C_{c2,n})},$$

$$\omega_{p2,n} = \frac{1}{R_{L1,n}(C_{L1,n} + g_{mn2,fb}R_{L2,n}C_{c1,n})},$$

$$\omega_{p3,n} = \frac{1}{R_{L3,n}(C_{L3,n} + C_{c2,n})},$$

$$\omega_{z1,n} = \frac{1}{C_{c2,n}\left(\frac{1}{g_{mn3,fb}} - R_{z,n}\right)},$$

$$\omega_{z2,n} = \frac{g_{mn2,fb}}{C_{c1,n}},$$

$$A_{v,DC} = \frac{1}{2} \cdot \frac{g_{mn1,fb}g_{mn2,fb}g_{mn3,fb}R_{L1,n}R_{L2,n}R_{L3,n}}{(1 + g_{mn1,fb}R_s)} \tag{13}$$

$$\omega_{p1,p} = \frac{1}{R_{L2,p}(C_{c1,p} + g_{mp3,fb}R_{L3,p}C_{c2,p})},$$

$$\omega_{p2,p} = \frac{1}{R_{L1,p}(C_{L1,p} + g_{mp2,fb}R_{L2,p}C_{c1,p})},$$

$$\omega_{p3,p} = \frac{1}{R_{L3,p}(C_{L3,p} + C_{c2,p})},$$

$$\omega_{z1,p} = \frac{1}{C_{c2,p}\left(\frac{1}{g_{mp3,fb}} - R_{z,p}\right)},$$

$$\omega_{z2,p} = \frac{g_{mp2,fb}}{C_{c1,p}},$$

$$A_{v,DC} = \frac{1}{2} \cdot \frac{g_{mp1,fb}g_{mp2,fb}g_{mp3,fb}R_{L1,p}R_{L2,p}R_{L3,p}}{(1 + g_{mp1,fb}R_s)} \tag{14}$$

$$A_{v,n} \approx \frac{1}{2} \cdot \frac{1}{(1 + g_{mn1,fb}R_s)} \cdot \frac{g_{mn1,fb}g_{mn2,fb}g_{mn3,fb}R_{L1,n}R_{L2,n}R_{L3,n}}{\left(1 + sR_{L2,n}(C_{c1,n} + g_{mn3,fb}R_{L3,n}C_{c2,n})\right)} \tag{15}$$

$$A_{v,p} \approx \frac{1}{2} \cdot \frac{1}{(1 + g_{mp1,fb}R_s)} \cdot \frac{g_{mp1,fb}g_{mp2,fb}g_{mp3,fb}R_{L1,p}R_{L2,p}R_{L3,p}}{\left(1 + sR_{L2,p}(C_{c1,p} + g_{mp3,fb}R_{L3,p}C_{c2,p})\right)} \tag{16}$$

$$A_v = A_{v,n} + A_{v,p} \approx \frac{1}{(1 + g_{mn1,fb}R_s)} \cdot \frac{g_{mn1,fb}g_{mn2,fb}g_{mn3,fb}R_{L1,n}R_{L2,n}R_{L3,n}}{\left(1 + sR_{L2,n}(C_{c1,n} + g_{mn3,fb}R_{L3,n}C_{c2,n})\right)} \tag{17}$$

Table 5 is the OPAMP simulation results. The OPAMP open-loop gain is 59.9 dB and its phase margin is 65°. Fig. 11 shows that the OPAMP is designed as a single pole system within the GBW. Fig. 12 shows the CMFB loop stability. Because of the second zero and third pole, the phase decreases rapidly in the band over GBW. Both phase margins cover 60°, with any value over that meaning the circuit is stable. The complementary structure and common source of the second stage take advantage of large the input/output signal. Fig. 13 shows good linearity, in that OP1dB is 4.9 dBm.

3. Source Follower

The source follower is described in Fig. 14. The structure consists of two cascaded amplifiers, which are the current mirror load OTA (operational transconductance amplifier) and the common source with the diode connected load. Because of the

Table 5. Simulation results of OPAMP

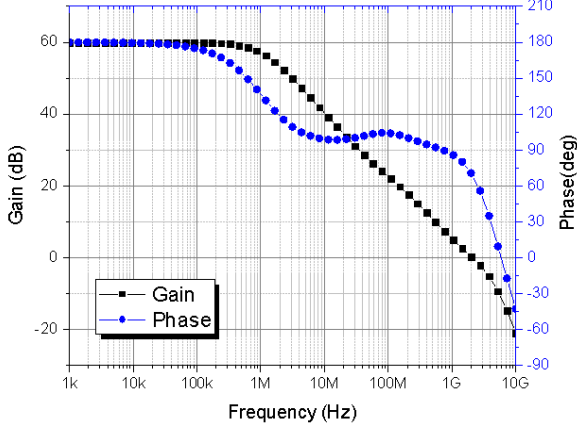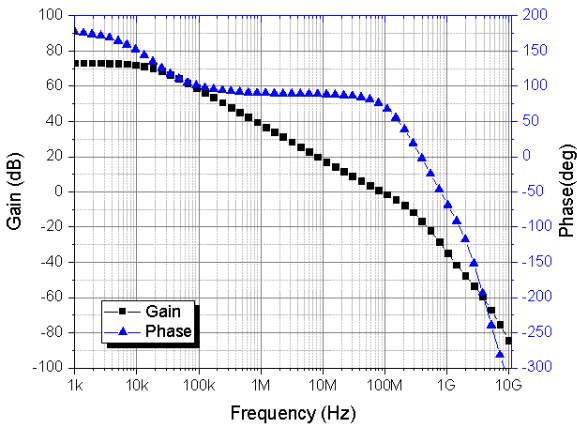| Parameter	Value
Open loop gain	59.9 dB
Open loop phase margin	65°
GBW	2.3 GHz
Current	5.3 mA
CMFB gain	73 dB
CMFB phase margin	73°
OP1dB	4.9 dBm
OIP3	22 dBm

Fig. 11. Proposed OPAMP transfer function.
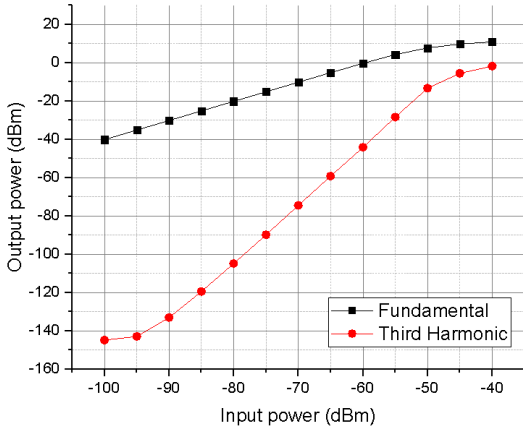

Fig. 12. CMFB loop stability.

Fig. 13. OPAMP linearity.

diode-connected-load at the output node, the circuit is subject to low output impedance. The feedback path of 1 with feedback factor β makes the 3 dB frequency the same is the unit gain frequency; the output node of the OTA is the dominant pole. This is like a unit gain buffer with low output impedance. The SF also consists of a complementary structure. The P-type and N-type SF operate in other saturation regions (Fig. 15). The SF open-loop transfer function is shown Eq. (18).
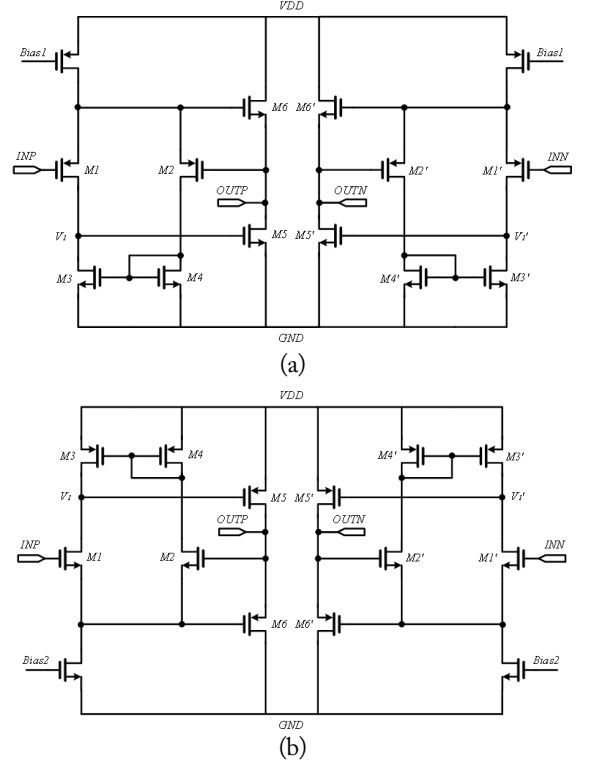

(a)

(b)

Fig. 14. Source follower schematic: (a) PMOS source follower and (b) NMOS source follower.
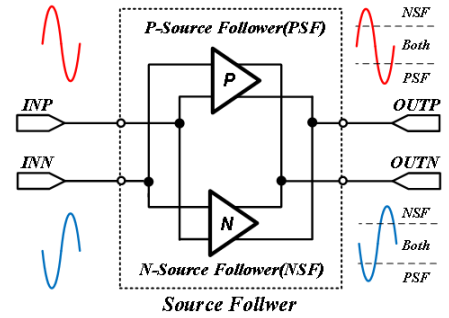

Fig. 15. Complementary source follower block diagram.

$$\therefore A_{v,SF\ Open} = \left(\frac{g_{m1}(r_{o2}\|r_{o4})}{(1 + s\omega_{V_{p1}})} \cdot \frac{-g_{m5}}{g_{m6}} \right)_{NSF}$$

$$+ \left(\frac{g_{m1}(r_{o2}\|r_{o4})}{(1 + s\omega_{V_{p1}})} \cdot \frac{-g_{m5}}{g_{m6}} \right)_{PSF} \tag{18}$$

where $s\omega_{V_{p1}}$ is the first pole at node V_1.

Figs. 16 and 17 show the transfer functions (including that of the DC). The exact description of the SF has been explained elsewhere [10]. Table 6 presents the SF's simulation results. Low output impedance driving causes two features. First, the output node pole is in the high frequency band. As a result, the SF has only single pole system in an operating frequency band. Second, the output node requires a 50 Ω driving current. The output's
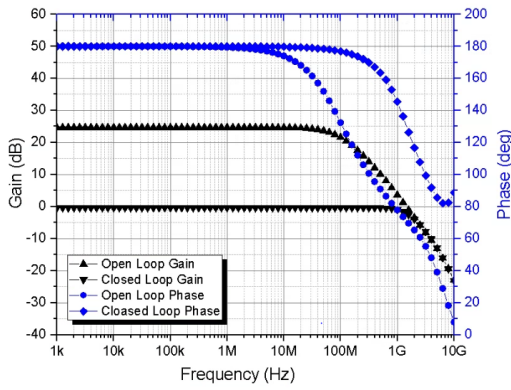
Fig. 16. Simulated source follower transfer function.

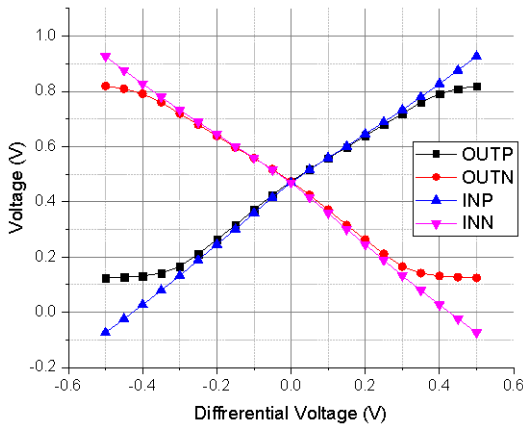Fig. 17. Simulated source follower DC transfer function.

Table 6. Simulation results of source follower

Parameter	Value
Gain	−0.6 dB
Phase margin	131°
GBW	1.09 GHz
Current	11 mA

common mode voltage should maintain VDD/2 with 50 Ω load impedance. As a result, a large DC current is needed in circuit.

III. SIMULATION AND EXPERIMENT RESULTS

The filter is fabricated in a CMOS 65 nm process. The chip of the area is 0.18 mm², as shown in Fig. 18(a). The measurements are implemented as follows:
- The designed filter is set by wire bonding on printed circuit board (PCB),as shown in Fig. 18(b).
- The differential input signal is made by a balun, which makes single to differential signal, this covers 6.5 MHz to 4 GHz.
- Input and output impedance are matched at 50 Ω by the R and, C elements on the PCB. The output node is connected to the spectrum analyzer (E4440A) and oscilloscope.
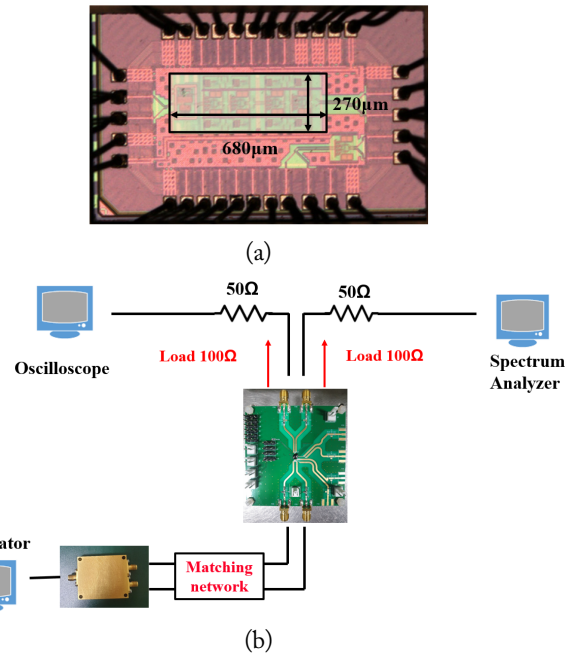

Fig. 18. (a) Die photo and (b) test environment for measurement.

- Passed signal after balun is nominated input signal.

With the CMFB circuit, not only could the output DC of the two-stage differential OPAMP block unwanted noises from the supply or ground, but the output voltage will also follow a reference voltage, as shown in Fig. 19. The measured 3-dB frequency is 330–630 MHz. Compared with the simulated 3-dB frequency, there is a small difference (simulated result 384–681 MHz). The 3-dB frequency is tuned by tunable capacitor C ($C = C_1 = C_2$, in Fig. 3) The simulated and measured transfer function is shown in Fig. 20. In the in-band area, the ripple is 2.5 dB. The filter 3-dB cutoff frequency does not seem to be degraded by the SF, because the SF's GBW which is 1.09 GHz, covers the filter's transfer function. The linearity measurement is implemented at the main tone of 100 MHz and another tone of 110 MHz. The two-tone test measurement is shown in Fig. 21. The simulated OIP3 is 11.7 dBm,
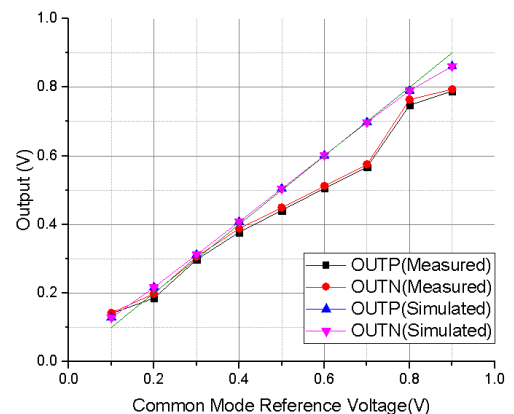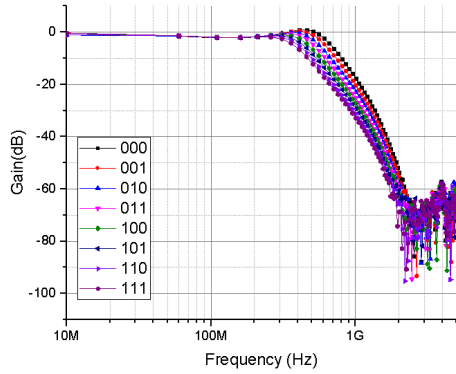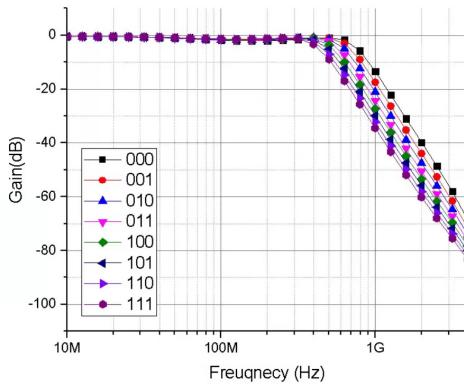

Fig. 19. Reference voltage vs output DC voltage.

(a)

(b)

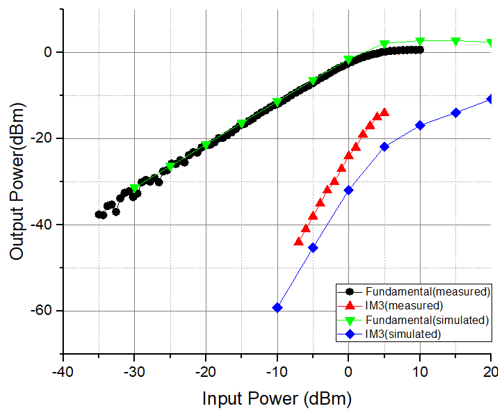Fig. 20. (a) Measured LPF transfer function and (b) simulated LPF transfer function.
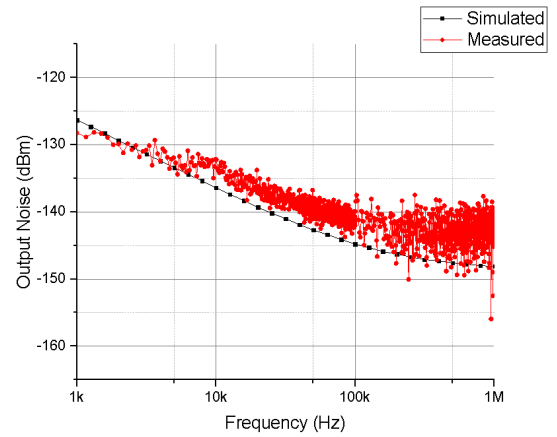

Fig. 21. Linearity of the LPF.

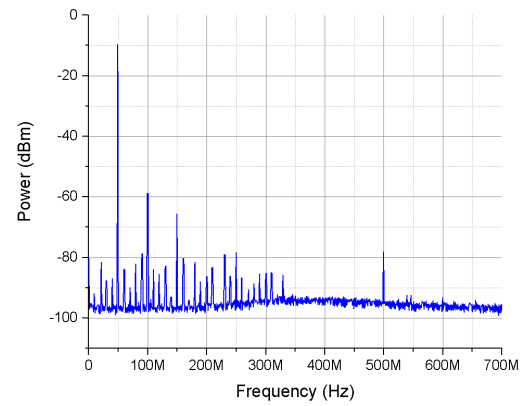Fig. 22. Output noise of the LPF.

Fig. 23. THD measurement of the LPF.

and the OP1dB is 0.7 dBm (differential zero to peak value). The measured OIP3 is 8.45 dBm and OP1dB is −1.3 dBm. The measured differences from simulation are 3.25 dB in OIP3 and 2 dB in OP1dB, because there are losses when implementing the mask layout and measurement environment.

Fig. 22 shows the output noise of the filter. Because the gain is 0 dB, the input referred noise (IRN) could be equal to the output noise, Fig. 23 shows the total harmonic distortion (THD); after the −10 dBm input signal at 50 MHz passes the LPF, the measured THD is −44.6 dB. Table 7 compares the specifications of this work with those of recently published papers [11–13].

Table 7. Summary of this work with recent other works

Study	Technology (mm)	Order type	Supply (V)	3dB-BW (MHz)	Power (mW)	Area (mm²)	Power/ pole (mW/Hz)	OIP3 (dBm)	OP1dB (dBm)	SFDR (dB)	THD (dB)	IRN (nV/$\sqrt{Hz}$)
This work	65	4	1	330–660	27	0.18	6.75	8.45	−0.7	49.1	−44.6	38.2
D'Amico et al. [11]	28	3	0.9	132	0.34	0.008	0.11	5.5	3	–	-30	–
Ye et al. [12]	180	6	1.8	240–500	0.47	0.23	3.86	1.25	–	48.8	–	13.1
Saari et al. [13]	65	5	1.2	275	36	0.21	7.2	10	–	–	–	7.8

IV. Conclusion

As a wideband LPF for the new 5G standard needs to be designed, this paper presents a wideband active R-C LPF with large GBW and complementary structured OPAMP in a 65 nm CMOS process. In the active R-C filter design, the performance of OPAMP is the most crucial point. The GBW of the OPAMP should be much larger than the 3-dB frequency of the LPF. In this system, there is a trade-off between bandwidth and current consumption. Because of the complementary two-stage structure, the proposed filter has a larger input/output signal range. Also, because the sensitive output impedance of the LPF should be isolated from low output impedance, an SF circuit needs to be inserted into the circuit. However, because the SF drives 100 Ω impedance without degrading linearity, the current consumption of the SF is nearly 11 mA. If there is a condition to drive large impedance in some applications, the current of the SF can be significantly reduced. Without the SF, the filter current consumption is 16 mA. Another advantage of the proposed filter is a wide variable range from 330 MHz to 660 MHz with a low THD of -44.6 dB. Compare with recent papers, the proposed circuit operates at low supply voltage and wide bandwidth.

References

[1] 3GPP, "TS 38.101-2 V17.2.0," 2021 [Online]. Available: https://portal.3gpp.org/desktopmodules/Specifications/SpecificationDetails.aspx?specificationId=3284.

[2] S. D'Amico, M. De Blasi, M. De Matteis, and A. Baschirotto, "A 255 MHz programmable gain amplifier and low-pass filter for ultra low power impulse-radio UWB receivers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 2, pp. 337-345, 2012.

[3] H. Elwan, A. Tekin, and K. Pedrotti, "A differential-ramp based 65 dB-linear VGA technique in 65 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 9, pp. 2503-2514, 2009.

[4] S. Kumaravel, B. Venkataramani, S. Rishi, V. S. Vijay, and B. Shailendra, "An enhanced folded cascode OTA with push pull input stage," in *Proceedings of International Multi-Conference on Systems, Signals & Devices*, Chemnitz, Germany, 2012, pp. 1-6.

[5] S. Zhang, Z. Zhu, H. Zhang, Z. Xiong, and Q. Li, "A 90-dB DC gain high-speed nested gain-boosted folded-cascode opamp," in *Proceedings of 2015 11th Conference on Ph. D. Research in Microelectronics and Electronics (PRIME)*, Glasgow, UK, 2015, pp. 357-360.

[6] F. Roewer and U. Kleine, "A novel class of complementary folded-cascode opamps for low voltage," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 8, pp. 1080-1083, 2002.

[7] Q. Zhou, H. Li, X. Duan, and C. Yang, "A two-stage amplifier with the recycling folded cascode input-stage and feedforward stage," in *Proceedings of 2011 Cross Strait Quad-Regional Radio Science and Wireless Technology Conference*, Harbin, China, 2011, pp. 1557-1560.

[8] P. M. VanPeteghem and J. F. Duque-Carrillo, "A general description of common-mode feedback in fully-differential amplifiers," in *Proceedings of the IEEE International Symposium on Circuits and Systems*, New Orleans, LA, 1990, pp. 320-312.

[9] Y. Xin, X. Zhao, B. Wen, L. Dong, and X. Lv, "A high current efficiency two-stage amplifier with inner feedforward path compensation technique," *IEEE Access*, vol. 8, pp. 22664-22671, 2020.

[10] G. Xing, S. H. Lewis, and T. R. Viswanathan, "Self-biased unity-gain buffers with low gain error," *IEEE Transactions on Circuits And Systems II: Express Briefs*, vol. 56, no. 1, pp. 36-40, 2009.

[11] S. D'Amico, M. De Matteis, A. Donno, and A. Baschirotto, "A 0.9 V 3rd-order single-opamp analog filter in 28 nm bulk-CMOS," *Analog Integrated Circuits and Signal Processing*, vol. 98, pp. 155-167, 2019.

[12] L. Ye, C. Shi, H. Liao, R. Huang, and Y. Wang, "Highly power-efficient active-RC filters with wide bandwidth-range using low-gain push-pull opamps," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 1, pp. 95-107, 2013.

[13] V. Saari, M. Kaltiokallio, S. Lindfors, J. Ryynanen, and K. A. Halonen, "A 240-MHz low-pass filter with variable gain in 65-nm CMOS for a UWB radio receiver," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 7, pp. 1488-1499, 2009.

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